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PROGRAMMABLE ASYNCHRONOUS SINGLE LINE ADAPTER (PASLA) PROGRAMMING MANUAL

INTERDATA®
Subsidiary of PERKIN-ELMER
Oceanport, New Jersey 07757, U.S.A.

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INTRODUCTION

This manual contains a description of the Programmable Asynchronous Single Line Adapter (PASLA) and the information necessary to program the system. The PASLA provides an interface between a Multiplexor Bus or Selector Channel and a wide variety of modems and terminals in either the 2-wire or Half-Duplex (HDX) or the 4-wire or Full Duplex (FDX) mode. Because of the wide variety of modems and terminals available, the potential user must determine the suitability of the PASLA for his given application and network.

The PASLA is contained on a single 7" Printed Circuit board and contains the interface for one 2-wire or 4-wire line. Each line has two consecutive addresses, an even address for the Receive side and an odd address for the Transmit side. If strapped for 2-wire mode, both sides respond to either address, however standard practice is to use the even address. There is an Interrupt flip-flop associated with each side. Each 2-wire or 4-wire line can be programmed to adapt the character format and baud rate to a wide variety of data sets and their associated terminals.

The following documents are useful references to the PASLA user:

EIA RS-232C Standard (Electronic Industries Association)
202C/202D Data Set Interface Specification (AT&T)
103A Data Set Interface Specification (AT&T)
PASLA Maintenance Manual, INTERDATA Publication Number 29-307

CONFIGURATION

This Adapter can be used on any INTERDATA 16-Bit or 32-Bit Processor.

DATA FORMAT

Specifications

The following is a list of the salient PASLA specifications:

1. Baud Rates – The selected baud rate is obtained by a combination of a potentiometer adjustment and straps to yield a range from approximately 9600 to 50 baud. The baud rate may be programmed for one-out-of-two. These two baud rates are restricted to binary multiples of each other.

2. Character Format – The following three independent variables on the Character Format are programmable:

   Character Size – 5, 6, 7, or 8 data bits.
   Parity – Odd, even, or none.
   Stop Bits – One or two.

3. RS-232C Interface.

VOLTAGE	BINARY	SIGNAL LINE	CONTROL
+5V TO +15V	0	SPACE	ON
–5V TO –15V	1	MARK	OFF

4. Data Set Control (Programmable)

   a. Data Terminal Ready (CD) – Program control is provided over CD to provide for automatic call reception, disconnect, and lockout.

NOTE

Parenthesis indicate RS-232C designations for indicated functions.

   b. Reverse Channel Transmit (SA)* – Permits a supervisory signal to be transmitted over a secondary data path while simultaneously receiving data.

   c. Request to Send (CA) -- Active to maintain the Adapter in the Transmit mode. In HDX operation, the inactive state maintains the adapter in the Receive mode.

   d. Data Terminal Busy* – Enables the "Make Busy" feature when available.

5. Data Set Status – The following lines from the data set effect the status bits: CLEAR TO SEND (CB), CARRIER (CF), RING (CE), REVERSE CHANNEL RECEIVE (SB), and DATA SET READY (CC).

6. Echoplex – A programmable feature to transmit received data back to the data set in addition to assembling the character.

7. Other features – The PASLA provides a double-buffered character to permit a full character "grab time". The Start bit is automatically generated and transmitted by the hardware and, in the Receive mode, the Start bit must be present for at least one half bit time before the character assembly commences, thereby reducing the noise susceptibility of the system.

8. Method of Transmission – Serial, asynchronous by character, synchronous by bit.

9. Distortion:

   Transmit – The transmit data distortion shall be $\leq +3\%$ per character.

   Receive – The PASLA adjusts the data sampling strobe with each character received and tolerates a data bit distortion of ±40%. In addition, the long term transmission rate may vary by ±5%. The above assumes that the Baud Rate Adjust potentiometer is adjusted accurately. See 02-279A21, provided in the *PASLA Maintenance Manual,* Publication Number 29-301.

Transfer Format

Asynchronous operation requires that all characters be preceded by one Start bit (=0) and have at least one Stop bit (=1) appended after the last data bit or the Parity bit, if selected. The Start and Stop bits delineate characters. A typical format for the Teletypewriter (110 Baud) is shown in Figure 1.

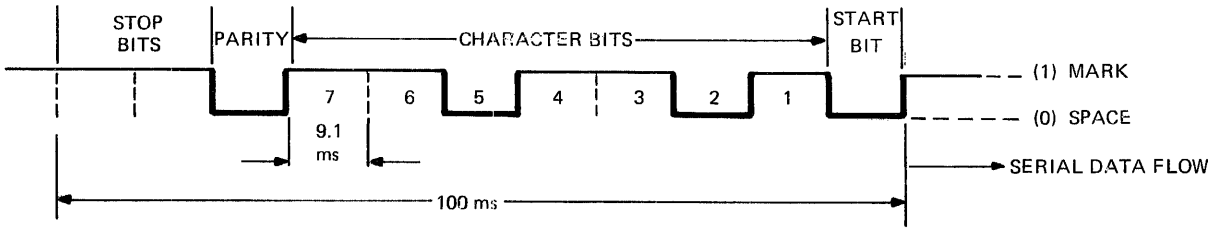


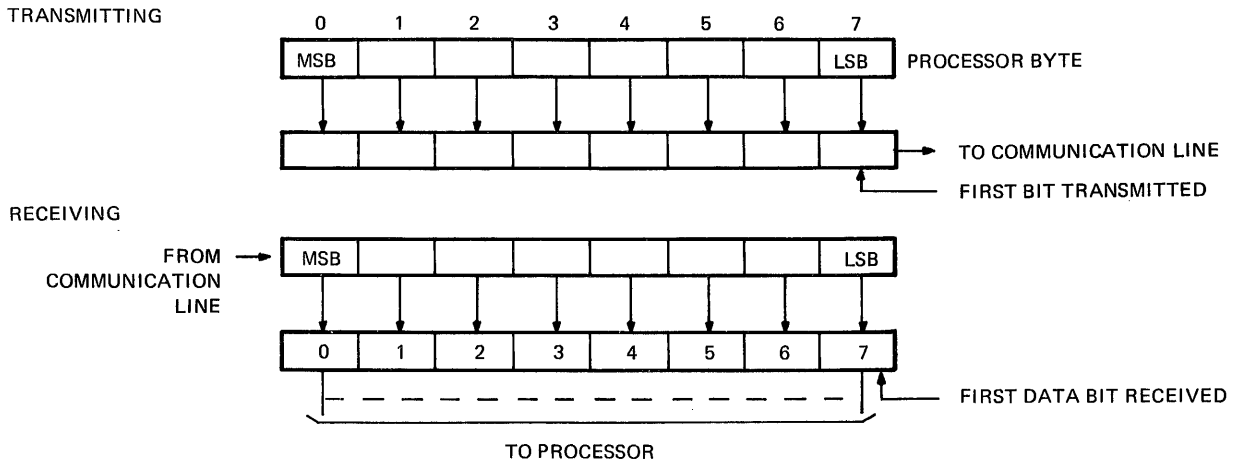
Figure 1 Typical ASCII Character Format

Note that, in this example, to send seven useful bits of information, eleven code elements (bits) are required. Therefore, to send 70 bits of useful information per second, the system must operate at 110 baud.

The single Start bit is generated by the hardware, and the character size/parity and number of Stop bits are under program control.

*Optional features in some data sets.

Order of Transmission



NOTE

There are terminals which require the MSB to be transmitted (or received) first. For such terminals the data should be presented by the program (or will be presented by the PASLA) with the MSB of data in Position 7 of the Processor byte.

PROGRAMMING INSTRUCTIONS

The Processor I/O instructions are used to communicate with the PASLA. The following paragraphs describe how Processor I/O instructions may be used with the system.

PASLA Program Instructions

Sense Status (SS or SSR)

The Sense Status instruction is used to determine if character transfers are complete and correct, and to interrogate the associated data set status.

Output Command (OC or OCR)

The Output Command instruction is used to answer or disconnect calls, to set the PASLA in the Receive or Transmit mode, and to select the character format. Two Command bytes are required to perform these functions.

Write Data (WD or WDR)

The Write Data instruction is used to load the output character into the PASLA Data Register.

Read Data (RD or RDR)

The Read Data instruction is used to read an assembled character into the Processor.

Acknowledge Interrupt (AI or AIR)

The Acknowledge Interrupt instruction is used to service interrupts. Execution of this instruction returns the address and status of an interrupting line. This instruction is used only for the 16-Bit Processors.

Communication Instructions

The PASLA accommodates the Communication instructions in the Communication Processors (Model 50, 55, 60).

Auto Driver Channel

The PASLA may be used with ADC on the 32-bit Processors.

Status and Command Bytes

Table 1 contains the PASLA Status and Command Byte Data.

TABLE 1. PASLA STATUS AND COMMAND BYTE DATA

BIT NUMBER / INSTRUCTION		0	1	2	3	4	5	6	7
PASLA STATUS		OV	PF or $\overline{CL2S}$	FR ERR	RCR	BSY	EX	CARR OFF	RING
PASLA COMMAND 1	RCV	DIS	EN	DTR	ECHO-PLEX	RCT or DTB	TRANS LB	WRT or RD	1
	SND	DIS	EN						
PASLA COMMAND 2		X	CLK	DATA BITS		STOP BIT	PARITY		0

X = Unused, must be ZERO.

PASLA STATUS

Refer to Figure 2 for PASLA – Data Set Communication lines.

OV* — The Overflow status bit is set to ONE if the previously received character is not read before the present character is assembled. Double-character buffering in the PASLA permits a full-character "grab-time". The Overflow status bit can be ONE in the Receive side only. It is reset at the next end of character, only if the failure condition disappears (i.e., is cleared by a Read Data instruction). The character causing Overflow is assembled and the previous character is lost.

PF* — In the Read mode, this bit is ONE when the received parity disagrees with the programmed parity. If parity is not selected via an Output Command, this bit remains ZERO. Once set, the PF status bit remains set until the failure condition disappears (i.e., a character with correct parity is assembled.)

$\overline{CL2S}$ — The lack of Clear to Send signifies that the modem can no longer transmit data. In the Write Mode, this status bit set indicates that Clear to Send (CB) is not being received from the data set. See Figure 2. This condition also forces BSY=1 on the Transmit Side. A Transition from $\overline{CL2S}$=0 to $\overline{CL2S}$=1 causes an interrupt if enabled.

FR ERR* — The Framing Error status bit is set to ONE to indicate that the received character has no Stop bit(s). That is, the line is in the SPACE state instead of the MARK state at Stop Bit time. If the character has two Stop Bits, only the first is tested, and the character assembly terminates after the first Stop Bit. In the case of a Framing Error, the character is assembled. A ZERO character can signify the beginning of a line break sequence. In the case of a line break (prolonged SPACE), if the line remains spacing, only the first character is assembled. Subsequent SPACE characters are not assembled until a MARK to SPACE transition is received. Note that because of this characteristic where the line break facility is being employed, a line break decision must be based on a single ZERO character with Framing Error. Once set, this bit remains set until the assembly of a character with a Stop Bit.

RCR — REVERSE CHANNEL RECEIVE (SB)* is an option in some half-duplex data sets (e.g., 202C). This status bit is set if the Reverse Channel Line from data set is ON. This bit is reset if the Reverse Channel Line from data set is OFF. If the data set does not have the Reverse Channel option, this status bit is always inactive. Either transition of this signal causes an interrupt, if enabled.

BSY = 1 when,

1. Data Set Ready (CC) from the data set is OFF (EX=1).
2. Character is not assembled in Read mode.
3. Clear to send (CB) is OFF ($\overline{CL2S}$=1) in Write mode.
4. When the interface has not yet transmitted the last character in the Write mode.

BSY = 0 when the interface is able to transfer data in Read/Write mode.

An interrupt is generated, if enabled, when BSY changes from 1 to 0.

In the Read mode, when an overflow occurs, the BSY status bit is reset to ZERO and a Read Data instruction must be issued to set the Busy bit to its correct (ONE) state.

*These status bits are set at End of Character time when the BUSY Bit is ZERO. Since the resetting of BUSY causes an interrupt (if enabled), these bits do not generate individual interrupts. At this point a Read Data instruction must be issued to set the Busy bit.

EX — EXAMINE=OV+PF+$\overline{\text{DATA SET READY}}$ + FRERR. This bit is disabled in FDX on the Write side. Loss of Data Set Ready (DSRDY) cannot be detected on the Write side in FDX operation. On the Receive side, $\overline{\text{DATA SET READY}}$ is indicated by Busy and Examine being ONE; other bits may also be ONE.

CARR OFF — CARR OFF is ONE to indicate that no valid incoming data is being received. In the Receive side, this bit is ONE to indicate that CARRIER (CF) is not being received from the data set (see Figure 2). In the Write mode, this status bit is ZERO when REQUEST TO SEND (CA) is active. A transition of this status bit in either direction causes an interrupt, if enabled.

RING — RING is ONE when the RING (CE) signal from the data set is active. This indicates the reception of a call. An interrupt is generated, if enabled, when RING changes to ONE. In 4-wire operation, RING is always ZERO on the Transmit (Send) side. The Ring status represents the present state of the equivalent data set signal. See Figure 2.

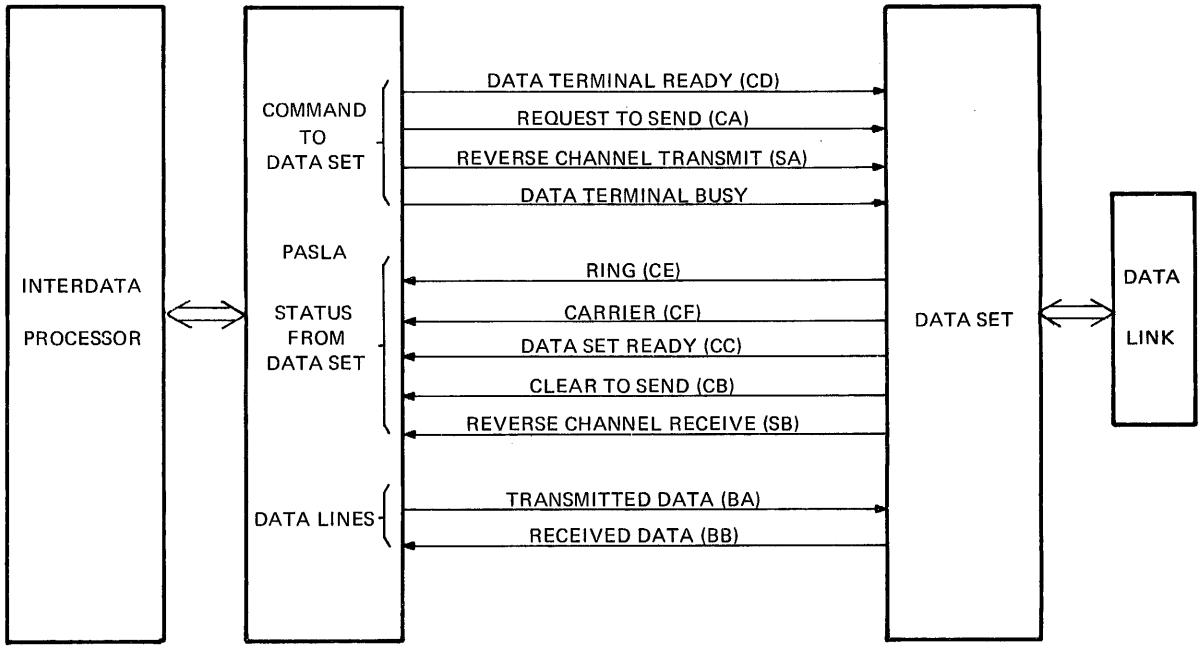


Figure 2. PASLA — Data Set Communication Lines

PASLA COMMAND 1 BITS

PASLA needs two 1-byte output commands.

In the PASLA Command 1, the DTR, ECHOPLEX, RCT/DTB, TRANS LB, and WRT/RD bits are shared by the Transmitter and Receiver. However, the EN/DIS bits are separate for Transmit and Receive sides.

DIS,EN

In 2-wire operation, the unused side interrupts remain disarmed. The used side interrupts can be enabled or disabled. In 4-wire operation, these bits must be independently programmed as follows. To change EN/DIS on the Receive side, issue a Command with the WRT/RD bit = 0. To change the EN/DIS on the Transmit side, issue a Command with the WRT/RD bit = 1. The WRT/RD bit is gated to the data set as REQUEST TO SEND. Therefore, in 4-wire operation, it is essential that a command with WRT/RD = 0 be followed with a command WRT/RD = 1 in order to insure that REQUEST TO SEND does not deactivate.

DISABLE	ENABLE	
0	0	No Change
0	1	Enable
1	0	Disable (Interrupt queued)
1	1	Complement (Change state)

DTR

DATA TERMINAL READY (CD) to the data set. When this command bit is set, CD is turned ON, allowing automatic answering of an incoming call. This line must be ON to permit the data set to enter and remain in the data mode. When this bit is reset, it does not permit automatic answering of an incoming call and causes an existing connection to disconnect if held reset for a period specified by the manufacturer of the data set. See Figure 2.

ECHO-PLEX

When this bit is set, data received from the data set is transmitted back to the data set on the TRANSMITTED DATA (BA) line. See Figure 2. The PASLA also assembles the character as in the normal data mode. This feature is normally used for 4-wire HDX operation in the Read mode to provide visual verification at the terminal of the data received by the computer. This command must not be issued to the transmit side. Note that in the 2-wire HDX Read mode the RQ2S line is not active. If the associated data set requires RQ2S to be active, the data will not pass to the communication link. This bit takes effect immediately. Therefore, a Write to Read (with Echo-Plex) mode change requires transmitting X'FF' (an ASCII DEL character) as the last character.

RCT/DTB

RCT (Reverse Channel Transmit) (SA) is optional on 202C-type data sets, DTB (Data Terminal Busy) is optional on 103-type data sets. See Figure 2. For Reverse Channel Transmit option, this command bit is gated directly to the Secondary Transmitted Data (SA) line. See Figure 2. When this bit is set, RCT is OFF, i.e. Reverse Channel is not transmitted. When this bit is reset, RCT is ON, i.e. Reverse Channel is transmitted. For data sets equipped with the Data Terminal Busy option, the reset condition of this command bit will "busy-out" the terminal thereby not allowing a call to be answered and returning the Busy signal to the calling terminal.

TRANS LB

When this bit is set, a continuous SPACE is transmitted to the data set. This condition overrides the Echo-plex feature. If this command is issued while data is being transmitted, the transmitted data will be mutilated.

WRT/RD

This command bit controls REQUEST TO SEND (CA) to the data set. See Figure 2. When this bit is set, REQUEST TO SEND is gated to the data set if DATA SET READY* (CC) is active. When this bit is reset, the hardware deactivates REQUEST TO SEND (CA) after the following delays: If character transfers are in progress, the hardware insures that the last character has been transmitted, then delays one millisecond to permit the last data bit to clear the data set before dropping REQUEST TO SEND (CA) except as noted under ECHO-PLEX. BSY is set during this line turn-around and does not reset until a character is received. However, CL2S, CARR OFF, RING, RCR, and DSRDY may still generate interrupts, if enabled. See Figures 3 and 4. In 2-wire operation, setting this bit places PASLA in the Write mode; resetting this bit places PASLA in the Read mode. In 4-wire operation, this bit is normally programmed set except noted under DIS, EN above.

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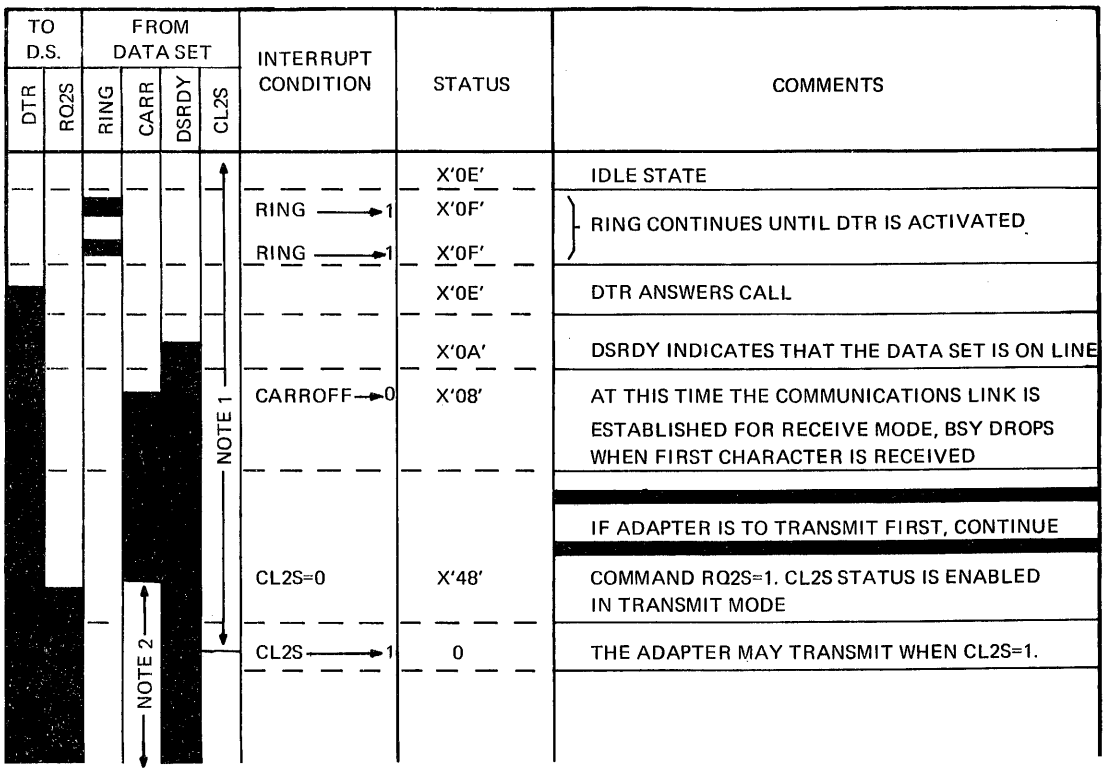
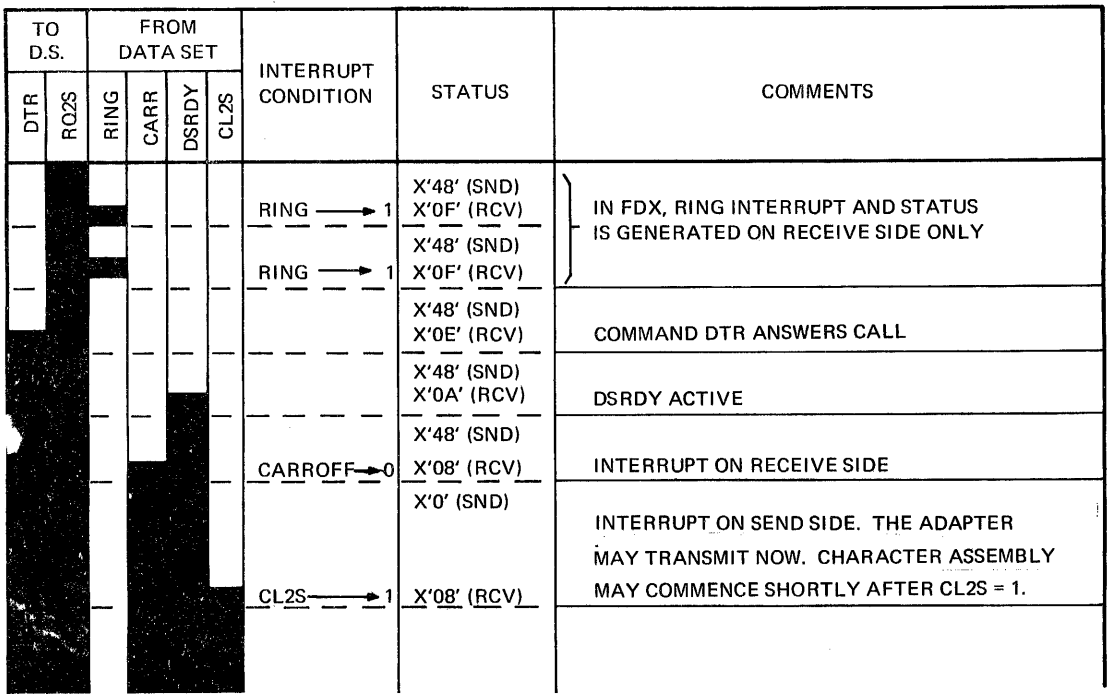
*DATA SET READY (CC) does not appear in the status byte on the Transmit side in FDX operation. It should be noted here that one must rely on the receive side of the adaptor for notification of the loss of Data Set Ready (CC). Loss of Data Set Ready on the transmit side in FDX operation does not cause an interrupt. It does however hold Busy high thus preventing any more end of character interrupts.

(A) ANSWER CALL HDX MODE (202 – TYPE DATA SET)



NOTE 1: CL2S IS DE-ACTIVATED WHEN RQ2S = 0
NOTE 2: CARR IS DE-ACTIVATED WHEN RQ2S = 1 (CARR OFF = 0)
NOTE 3: THE STATUS SHOWN ONLY REFLECTS THE LINE CONDITIONS, NOT PF, OV, OR FR ERR. IN ADDITION REVERSE CHANNEL IS IGNORED SINCE THIS IS SUBJECT TO USER'S PROTOCOL.
NOTE 4: IF DTR IS SET WHEN RING OCCURS, THE CALL WILL BE ANSWERED AUTOMATICALLY (RING TERMINATES AND DSRDY BECOMES ACTIVE).

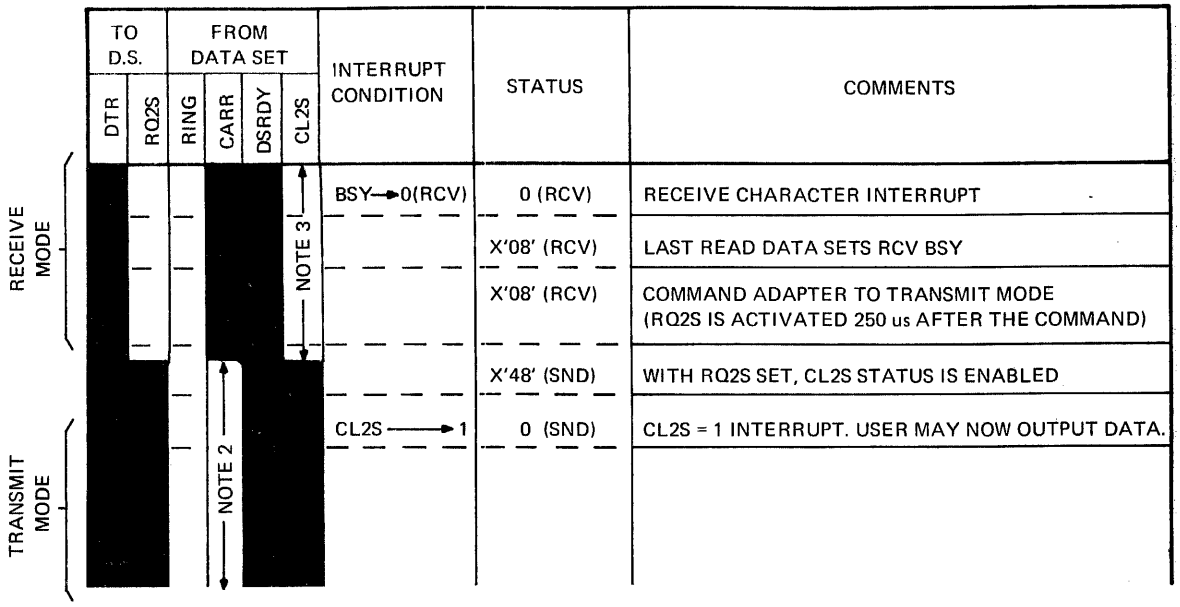
(B) ANSWER CALL FDX MODE (103 – TYPE DATA SET)



NOTE 1: CARR OFF AND DSRDY FORCED LOW ON TRANSMIT SIDE.
NOTE 2: REVERSE CHANNEL NOT APPLICABLE IN FDX (RCR = 0)

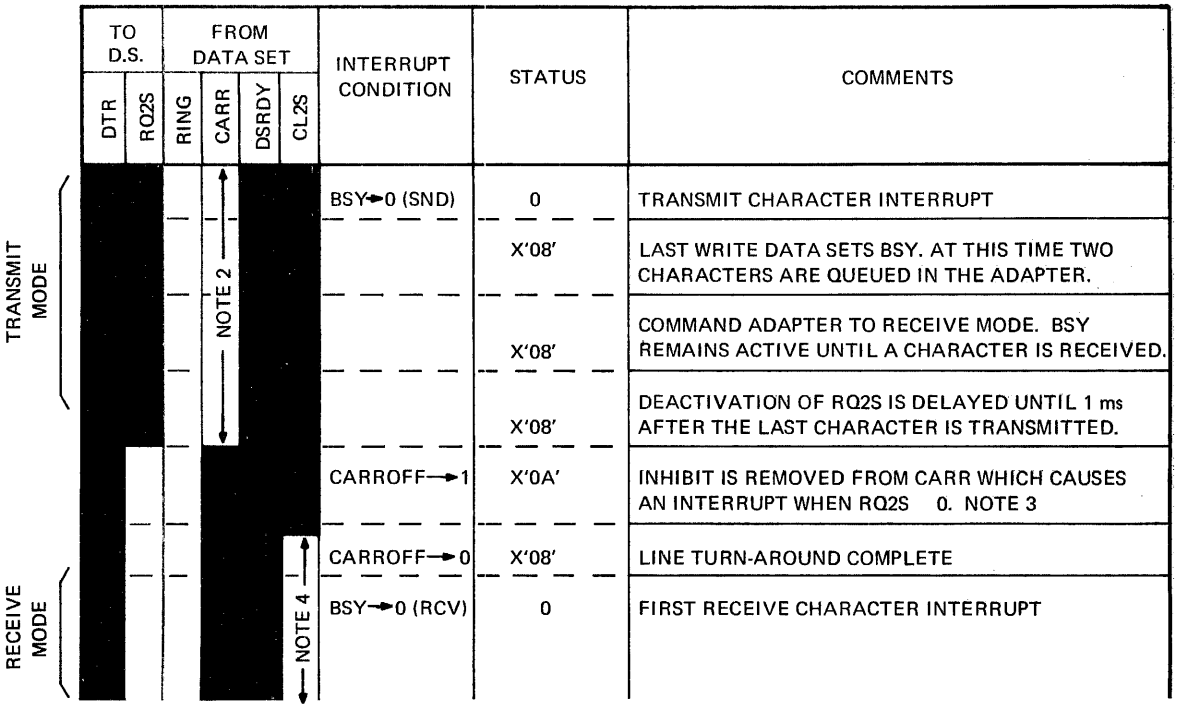
Figure 3. Answering Calls HDX and FDX

(A) LINE TURN–AROUND WRITE–READ (202 – TYPE DATA SET)



NOTE 1: INITIAL CONDITIONS; CONNECTION ESTABLISHED AND ADAPTER IS RECEIVING CHARACTERS.
NOTE 2: CARR OFF STATUS FORCED INACTIVE AND CARRIER INTERRUPTS INHIBITED.
NOTE 3: CL2S STATUS FORCED INACTIVE AND CL2S INTERRUPTS INHIBITED.

(B) LINE TURN–AROUND READ–WRITE (202 – TYPE DATA SET)



NOTE 1: INITIAL CONDITIONS: CONNECTION IS ESTABLISHED AND ADAPTER IS TRANSMITTING CHARACTERS.
NOTE 2: CARR OFF STATUS FORCED INACTIVE AND CARRIER INTERRUPTS INHIBITED.
NOTE 3: WITH A 103 TYPE DATA SET, CARRIER MAY BE PRESENT CONTINUOUSLY IN WHICH CASE THE CARROFF 1 INTERRUPT WILL NOT OCCUR AFTER DEACTIVATING RQ2S.
NOTE 4: CL2S STATUS FORCED INACTIVE AND CL2S INTERRUPTS INHIBITED.

Figure 4. Line Turn-Around Read/Write and Write/Read

PASLA COMMAND 2 BITS

CLK — CLK bit selects one of two strapped baud rates.

BIT #	1	CLOCK
	0	CLKA (Lowest Baud Rate)
	1	CLKB (Highest Baud Rate)

DATA BITS — DATA BITS select the number of data bits/character (not including parity)

BIT #	2	3	NO. OF DATA BITS
	0	0	5
	0	1	6
	1	0	7
	1	1	8

If fewer than eight data bits are selected when a Write Data is issued in the Write mode, the data must be right-justified and unused bits are "Don't Care". In the Read mode, when a Read Data is issued, the character is presented to the Processor right-justified with unused bits forced to the ZERO state.

STOP BIT — 0=1 Stop Bit
1=2 Stop Bits

When the line is programmed for two Stop bits, the PASLA Transmits both. However, the Receiver only samples the first Stop bit.

PARITY

BIT #	5	6	PARITY
	1	0	ODD
	1	1	EVEN
	0	X	NONE

In the Write mode, if parity is enabled (Bit 5=1), the PASLA generates and transmits the selected parity.

In the Read mode, if parity is enabled, the PASLA compares the received parity with the selected parity and generates the PF status if a disagreement is detected.

If parity is disabled (Bit 5=0), the hardware ignores parity. When transmitting, the hardware appends Stop bit(s) after the the last data bit and, when receiving, disables the Parity Detection Circuit.

NOTE

The least significant bit of the Command Byte must be a 1 or 0 as indicated to permit the hardware to distinguish between the two commands. Command 2 should never be issued while data transfer is in progress.

PROGRAMMING SEQUENCES

Switched Line Operation

To originate a call, the operator depresses the TALK key on the data set and dials the desired number. When the call is answered, a carrier is heard (being sent by the data set receiving the call). The operator then depresses the DATA key.

The operator may now hang up and depress the AUTO key to return the equipment to automatic receive following this call. When the DATA key is depressed (the Data Light remains lit for the duration of the call), the EX status bit resets (DATA SET READY) (CC) as does the CARR OFF status bit. The PASLA should be initialized to the Read mode and thus be interrupted by the receiving Carrier. When CARR OFF resets, the PASLA should be switched to the Write mode to transmit data. Following the call, both sets (originating and receiving) should be issued a Command Read with DTR reset to disconnect. This procedure is typical, but not necessary. The user is free to design his own hand-shake sequence. Figures 3 and 4 show timing sequences for answering calls and line turn-around. The following is offered for general information only. With wide variations between data set characteristics and common carrier procedures, the operating procedures may have to be modified. The user should ensure that the characteristics of the devices connected to the PASLA are compatible with the descriptions in this specification.

In Figure 3A, DTR and RQ2S are initially OFF. The status is X'0E' before RINGing commences. The RING causes an interrupt and a status of X'0F'. The RING status bit is set for the period of the RING from the data set.

When RING resets, the status is X'0E' and another interrupt is generated each time RING→1. RING continues until the program sets DTR to answer the call. Shortly after DTR is set, the data set responds with DSRDY=1. This causes EX→0 and the status at this time is X'0A' (BSY=1 and CARR OFF=1).

When the data link is established, the data set turns CARR ON which generates an interrupt and a status of X'08' (BSY=1). If the adapter remains in the Receive mode, Busy stays active until a character is received. If the adapter is to transmit first, the program turns RQ2S ON (Command with the WRT bit set). With RQ2S ON, the data set responds with CL2S=1. Since this bit is initially reset, an interrupt is generated when RQ2S is turned ON and another interrupt is generated when the data set responds with CL2S=1. The adapter may now transmit.

Figures 3 and 4 assume ideal conditions. For example, in a typical switched network environment, more than one interrupt may be generated as carrier is initially established, or the Received Data from the local data set may be active during a connect or disconnect sequence. These problems can be attributed to the type (manufacturer) of data set employed, the options implemented in the data set and also the switched network. In particular, if the Received Data from the data set is active before carrier is established, the PASLA will commence to assemble a "garbage" character. This can result in a Receive Busy interrupt with any or all of the character status bits set (PF, FRERR, OV). These status bits will then remain set until a Read Data is executed (to set BSY and reset OV) and a valid character is received (to reset PF and FRERR).

Leased Line Operation

In leased line operation, because a connection is permanently established, no dial-up or disconnect is needed. Both stations are normally initialized to the Read mode. Either end can originate a transfer by going into the Write mode, which causes the receiving station to interrupt when the Carrier appears. Upon receiving characters, the receiving end is in the Read mode, and a data transfer takes place. The exact hand-shake protocol is up to the user.

Half-Duplex Operation

In Half-Duplex operation, only one terminal can transmit at any one time. To change the direction of transmission, the channel must be turned around. The question arises as to who indicates channel turn-around. The convention is normally held that the Processor turns the line around when it has a message to transmit. Data sets (e.g. 202C type) normally used in Half-Duplex operation, may be equipped with the Reverse Channel option which is used to signal the requirement to reverse the direction of transmission or to break the data flow. An important operating convention affecting Reverse Channel operation results from the presence of echo suppressors in long-distance lines. These suppressors normally disallow transmission of an echo.

In data communications, the echo suppressor must be disabled, as it must be possible to transmit simultaneously in both directions (Main Channel and Reverse Channel). The echo suppressor becomes re-enabled if the tone on the line is absent for a period exceeding 100 milliseconds. To prevent the re-enabling of the echo suppressor, the convention should be adopted that the Reverse Channel is held ON (high) when the main channel is OFF and vice versa. This convention ensures that a tone is on the line at all times.

The Reverse Channel is normally held ON when the Processor is accepting data. The Processor signals its desire to transmit by lowering (OFF) the Reverse Channel and switching to the Write mode. A program delay should normally be introduced to allow the terminal on the other end to turn its Reverse Channel ON and enable its Read mode. This delay is a function of the terminal on the other end. This delay can be 200 to 1200 milliseconds. If the device at the other end is set up to indicate through the Reverse Channel signaling that it is ready to receive data, this can be used instead of a program delay. When the Processor is transmitting, a break condition sent from the terminal to signify that the terminal wants to transmit is signified by the Receive Reverse Channel going from ON (high) to OFF (low). The Processor should then raise its Reverse Channel lead high (ON) and transfer to the Read mode. The interface automatically introduces the necessary time delay before presenting data to the Processor to ensure valid data transfer and not transition noise.

Local Terminal Operation

As described above, the PASLA may be used in conjunction with modems to provide an Interface to a remote terminal. The PASLA contains the hardware to provide program control and status information at the RS-232 Interface.

The PASLA may also interface directly to asynchronous terminals which conform to the RS-232 specification. See Figure 5.

The major functional difference between the remote and local configuration shown in Figure 5 is that the local termination does not generally require the extensive hand-shaking sequences as described in the section on Switched Line Operation for switched network operation. Consequently, many of the standard RS-232 control and status lines are not terminated in the PASLA or the terminal for local connections. The nature of the Interface cannot be described specifically since it differs depending on the type of terminal. Typically, a CRT requires the Transmit and Receive Data paths to provide duplex operation and may also provide Data Terminal Ready for an on-line indicator to the PASLA. In either case, the local cable shown in Figure 5, combined with straps on the PASLA, will provide all of the features required to terminate most local terminals.

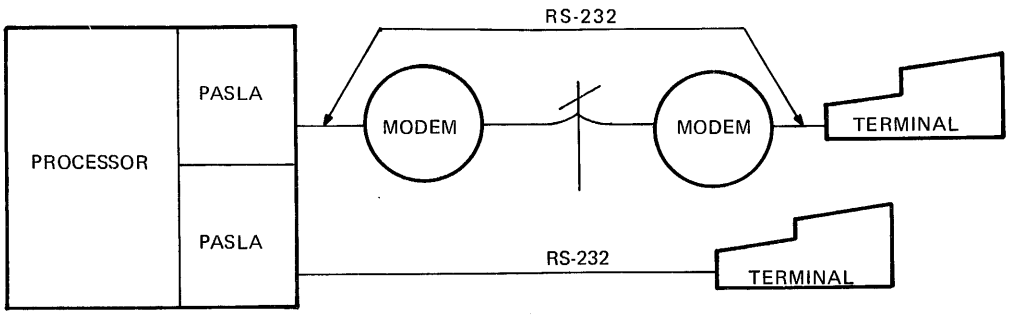


Figure 5. Local and Remote Terminal Connections

INTERRUPTS

A list of interrupt conditions is shown in Table 2.

TABLE 2. INTERRUPT CONDITIONS

STATUS BIT TRANSITION	HDX	FDX	
		REC	TRANS
RING ——→1	X	X	
CARR OFF ——→1	X (RD)	X	
CARR OFF ——→0	X (RD)	X	
RCR ——→1	X	X	
RCR ——→0	X	X	
DSRDY ——→0	X	X	
*BSY ——→0	X	X	X
$\overline{CL2S}$ ——→1	X (WRT)		X

* An interrupt is also generated in HDX operation when going from READ to WRITE mode if CL2S initially=0; i.e., when CL2S goes from 0 to 1 which causes a BSY interrupt.

INITIALIZATION

When the Initialize pushbutton on the Processor Display Panel is depressed (or after the power failure/restore sequence), OV, PF, and FR ERR status bits cannot be guaranteed. Because of this, the programmer should take precautions to ignore these bits on the first interrupt. The PASLA is placed in the Disable mode. A Read Data (RD or RDR) should be issued to set the BSY status bit.

The state of the command bits DTR, ECHOPLEX, RCT, TRANS LB and WRT/RD cannot be guaranteed when power is initially applied.

DEVICE NUMBER

The PASLA is normally strapped for X'10'.

Two consecutive addresses are assigned to each 4-wire line, with the even address for the Receive side and the odd address for the Transmit side. In 2-wire operation, each side responds to either address.

SAMPLE PROGRAMS

Programming Examples for 16-Bit Processor

Appendix 1 shows two examples. The first example is for Half-Duplex mode and data transfer is by use of Sense Status loops as well as under interrupts. The message 'TYPE 1234567890' is output using Sense Status loops. Then PASLA is put into the Read mode with Echo-plex enabled. A user input 10-character message is read using a Sense Status loop. When the complete message is received, the PASLA is put in the Write mode with interrupts enabled, and the message 'CORRECT!' is output under interrupts. The last Write interrupt is cleared.

The second example shows remote terminal 4-wire, switched-line operation. The data link connection, data transfer, and disconnect are under interrupt control. The user dials into the Processor. The example proceeds as Ring interrupts, DSRDY drops, and CARR OFF drops. When the user depresses a key on the remote terminal, BSY interrupts and a character is read into the buffer. A 10 character message is read in. Then RQ2S is sent to the PASLA. The modem responds with CL2S and BSY interrupts. Then same message is written to the terminal under interrupts. When complete, DTR is held off until DSRDY drops causing an interrupt. As the link is disconnected, CARR OFF sets, causing an interrupt. After some delay, CL2S sets causing an interrupt. BSY is also set. Thus, the line remains disconnected.

Programming Examples for 32-Bit Processor

The first example in Appendix 2 shows local terminal, 4-wire PASLA operation using Auto-Driver Channel for data transfer. A 10-character message is read from and written to the terminal. The example shows how to set up the interrupt service pointer table to use translation table and to check for proper Auto-Driver Channel termination.

The second example shows local terminal, 4-wire PASLA operation. The data transfer is under interrupt control. A 10-character message is read from and written to the terminal. The last Write side interrupt is cleared.

TESTING

The PASLA is tested using the PASLA Off-Line Test Program, 06-127, in conjunction with the 28-014 Test Connector. This requires two PASLAs. The test hardware and software are not delivered with the PASLA but may be purchased separately.

```
PASLA PROGRAMMING EXAMPLES FOR 16-BIT PROCESSOR          PAGE    1

PROG= *NONE*      03-066K05M96

                                1          SCRAT
                                2          CROSS
                                3          WIDTH  120
                                4  *
                                5  *  THESE EXAMPLES DEMONSTRATE SEQUENCES TO PROGRAM PASLA IN
                                6  *  VARIOUS ENVOIRNMENTS. THE TERMINAL & PASLA INTERFACE SHOULD
                                7  *  BE STRAPPED / CONNECTED AS MENTIONED IN INDIVIDUAL EXAMPLE.
                                8  *
                                9  * REGISTER ASSIGNMENTS
                               10  *
0000 0001                      11  MSG       EQU    1          MESSAGE START ADDRESS
0000 0002                      12  RCV       EQU    2          PASLA (RECEIVE) ADDRESS
0000 0003                      13  SND       EQU    3          PASLA (SEND) ADDRESS
0000 0004                      14  CHAR      EQU    4          CHARACTER BEING TRANSFERRED
0000 0005                      15  WORK      EQU    5          WORK REGISTER
0000 0006                      16  DONE      EQU    6          EXAMPLE DONE FLAG
0000 0007                      17  DEV       EQU    7          PASLA (HDX) ADDRESS
0000 0008                      18  STAT      EQU    8          PASLA STATUS
0000 0009                      19  REPEAT    EQU    9          EXAMPLE START ADDRESS
0000 000F                      20  LINK      EQU    15         LINK REGISTER
                               21  *
                               22  *
0000 0004                      23  EX        EQU    4          EX BIT IN STATUS BYTE IS ONE
0000 0008                      24  BSY       EQU    8          BSY BIT IN STATUS BYTE IS ONE
0000 0008                      25  CARRY     EQU    8          CARRY FLAG IN PSW IS ONE
                               26  *
```

LOCAL TERMINAL, HALF-DUPLEX PASLA OPERATION


```
                                    28  *
                                    29  *  TTY, CRT OR GDT SHOULD BE INTERFACED THROUGH PASLA(BSY) INTERFACE
                                    30  *  CRT/GDT SHOULD BE STRAPPED FOR HALF-DUPLEX OPERATION
                                    31  *  THE FOLLOWING EXAMPLE IS FOR 16-BIT PROCESSOR
                                    32  *  START EXECUTION @ START1
                                    33  *
                                    34  *  WRITE CHARACTERS & READ KEYS USING SENSE STATUS LOOP
                                    35  *  WRITE CHARACTERS UNDER INTERRUPT CONTROL
                                    36  *
                                    37  *
0000R  0766                         38  START1  XAR     DONE,DONE
0002R  9556                         39          EPSR    WORK,DONE           DISABLE INT @ PROCESSOR LEVEL
0004R  C890 0000R                   40          LDAI    REPEAT,START1
0008R  4870 0208R                   41          LH      DEV,DEVADR          GET PASLA DEVICE ADDRESS
000CR  DE70 020ER                   42          OC      DEV,SECOND          SET PASLA AS PER SECOND COMMAND
0010R  DE70 020FR                   43          OC      DEV,DISWRT          WRITE MODE
0014R  C810 0218R                   44          LDAI    MSG,MSG1            (MSG) = MESSAGE START ADDRESS
                                    45  *
0018R  D341 0000                    46  EXMP1A  LB      CHAR,0(MSG)
001CR  41F0 00A2R                   47          BAL     LINK,OUTCHR         OUTPUT A CHARACTER
0020R  2611                         48          AIS     MSG,1
0022R  C510 022AR                   49          CLAI    MSG,MSG1END
0026R  2087                         50          BLS     EXMP1A              LOOP TILL 'TYPE 1234567890' OUTPUTED
0028R  DE70 0210R                   51          OC      DEV,DISRD           SELECT READ MODE (ECHO-PLEX)
002CR  9B75                         52          ROR     DEV,WORK            DUMMY READ TO SET BSY
002ER  41F0 00AER                   53          BAL     LINK,DELAY          LINE TURN AROUND DELAY
0032R  0711                         54          XAR     MSG,MSG
                                    55  *
0034R  41F0 0092R                   56  EXMP1B  BAL     LINK,READ           READ A KEY CODE WHEN DEPRESSED
0038R  D441 021DR                   57          CLB     CHAR,TYPED(MSG)     COMPARE WITH THE EXPECTED
003CR  4230 003CR                   58          BNE     *
0040R  2611                         59          AIS     MSG,1
0042R  C510 000A                    60          CLAI    MSG,10
0046R  2089                         61          BLS     EXMP1B              LOOP TILL 10 DIGITS TYPED
                                    62  *
                                    63  * WRITE UNDER INTERRUPT CONTROL
                                    64  *
0048R  C850 006AR                   65          LDAI    WORK,INT
004CR  4060 0044                    66          STA     DONE,X'44'          SET UP NEW PSW FOR
0050R  4050 0046                    67          STA     WORK,X'46'          IMMEDIATE INTERRUPT
0054R  C810 022AR                   68          LDAI    MSG,MSG2
0058R  DE70 0211R                   69          OC      DEV,ENWRT           ENABLE INT @ PASLA LEVEL (1 PENDING)
005CR  41F0 00AER                   70          BAL     LINK,DELAY          LINE TURNAROUND DELAY
0060R  C850 4000                    71  EXMP1C  LDAI    WORK,X'4000'
0064R  9545                         72          EPSR    CHAR,WORK           ENABLE INT @ PROCESSOR LEVEL
0066R  4300 0066R                   73          B       *
                                    74  *
                                    75  * IMMEDIATE INTERRUPT IS RECEIVED
                                    76  *
006AR  9F58                         77  INT     AIR     WORK,STAT           ACKNOWLEDGE AN INTERRUPT
006CR  0557                         78          CLAR    WORK,DEV            COMPARE DEVICE THAT INTERRUPTED
006ER  4230 006ER                   79          BNE     *
0072R  0888                         80          LDAR    STAT,STAT           STATUS SHOULD BE ZERO (BSY = 0)
0074R  4230 0074R                   81          BNZ     *
```

LOCAL TERMINAL, HALF-DUPLEX PASLA OPERATION

```
0078R  0866                    82            LDAR    DONE,DONE
007AR  4230 00B6R              83            BNZ     HALT            HALT IF DONE
                               84    *
007ER  DA71 0000               85            WD      DEV,0(MSG)      WRITE A CHARACTER
0082R  2611                    86            AIS     MSG,1
0084R  C510 0238R              87            CLAI    MSG,MSG2END
0088R  4280 0060R              88            BL      EXMP1C          LOOP TILL 'CORRECT' OUTPUTED
008CR  2461                    89            LIS     DONE,1          SET DONE FLAG
008ER  4300 0060R              90            B       EXMP1C          ACKNOWLEDGE LAST INTERRUPT
                               91    *
                               92    *
0092R  9D78                    93    READ    SSR     DEV,STAT        SENSE PASLA STATUS
0094R  4240 00B6R              94            BTC     EX,HALT         HALT IF 'EX' IS SET
0098R  2083                    95            BTBS    BSY,3           LOOP IN 'BSY'
009AR  9B74                    96            RDR     DEV,CHAR        READ CHARACTER WHEN BSY DROPS
009CR  C440 007F               97            NAI     CHAR,X'7F'      REMOVE PARITY BIT
00A0R  030F                    98            BR      LINK            RETURN
                               99    *
00A2R  9D78                   100    OUTCHR  SSR     DEV,STAT
00A4R  2081                   101            BTBS    BSY,1           LOOP ON BSY
00A6R  9A74                   102            WDR     DEV,CHAR
00A8R  9D78                   103            SSR     DEV,STAT
00AAR  2081                   104            BTBS    BSY,1           WAIT FOR PASLA TO BECOME NOT BSY
00ACR  030F                   105            BR      LINK            RETURN
                              106    *
00AER  0755                   107    DELAY   XAR     WORK,WORK
00B0R  2651                   108            AIS     WORK,1
00B2R  2281                   109            BFBS    CARRY,1
00B4R  030F                   110            BR      LINK
                              111    *
00B6R  2451                   112    HALT    LIS     WORK,1          WORK = X'8000'
00B8R  915F                   113            SLHLS   WORK,15         HALT PROCESSOR
00BAR  9515                   114            EPSR    MSG,WORK
00BCR  0309                   115            BR      REPEAT
                              116    *
```

```
                                118  *
                                119  * PHONE RECEIVER IS IN IT'S CRADDLE
                                120  *
                                121  *
                                122  *
                                123  * START THE PROGRAM @ START2. DIAL IN THE PROCESSOR TELEPHONE
                                124  * NUMBER FROM THE TELETYPE TERMINAL. WHEN CARRIER IS HEARD,ENGAGE
                                125  * THE PHONE RECEIVER IN THE COUPLER. OBSERVE DATA SET LIGHTS TO
                                126  * MAKE SURE THAT CONNECTION IS ESTABLISHED. THE PROCESSOR SHOULD BE
                                127  * IN WAIT STATE. TYPE 10 CHARACTER MESSAGE ON TELETYPE. THE
                                128  * PROGRAM ECHOES BACK THE SAME MESSAGE & DISCONNECTS THE LINE.
                                129  * USER SHOULD REPLACE THE RECEIVER IN IT'S CRADDLE.
                                130  *
                                131  *
00BER  0766                     132  START2   XHR    DONE,DONE
00C0R  9516                     133           EPSR   MSG,DONE          DISABLE INT @ PROCESSOR LEVEL
00C2R  C810 010AR               134           LHI    MSG,INT1
00C6R  4060 0044                135           STH    DONE,X'44'        SET UP NEW PSW FOR IMMEDIATE INT.
00CAR  4010 0046                136           STH    MSG,X'46'
00CER  C890 00BER               137           LDAI   REPEAT,START2
00D2R  4820 0204R               138           LH     RCV,RCVADR        GET DEVICE ADDRESSES
00D6R  4830 0206R               139           LH     SND,SNDADR
00DAR  DE20 020ER               140           OC     RCV,SECOND        SET UP PASLA
00DER  DE30 0212R               141           OC     SND,DISWRT2
                                142  *
00E2R  9D38                     143           SSR    SND,STAT
00E4R  C580 0048                144           CLHI   STAT,X'48'        CLS NOT & BSY MUST BE SET
00E8R  4230 00E8R               145           BNE    *
00ECR  DE20 0213R               146           OC     RCV,ENREAD
00F0R  DE20 0214R               147           OC     RCV,WRTRD
00F4R  9B25                     148           RDR    RCV,WORK          DUMMY READ
00F6R  9D28                     149           SSR    RCV,STAT
00F8R  C480 001F                150           NHI    STAT,X'1F'        IGNORE OV,PE,FR ERROR AS THEY ARE
                                151  *                                  NOT GUARANTEED ON INITIALIZATION
00FCR  278E                     152           SIS    STAT,14           BSY,EX,CARR OFF MUST BE SET
00FER  4230 00FER               153           BNZ    *
0102R  C810 023AR               154           LHI    MSG,MSG4
0106R  C200 020AR               155           LPSW   WAIT
                                156  *
010AR  9F78                     157  INT1     AIR    DEV,STAT
010CR  0572                     158           CLHR   DEV,RCV
010ER  4230 010ER               159           BNE    *
0112R  C580 000F                160           CLHI   STAT,X'0F'        RING INTERRUPT
0116R  4230 0116R               161           BNE    *
011AR  DE20 0215R               162           OC     RCV,DTR           INDICATE DTR TO DATA SET,ECHO,DTB
011ER  C850 0134R               163           LHI    WORK,INT3
0122R  4050 0046                164           STH    WORK,X'46'
                                165  *
0126R  9D28                     166  SENSE2   SSR    RCV,STAT
0128R  C580 000A                167           CLHI   STAT,X'0A'        DATA SET READY SHOULD DROP
012CR  2033                     168           BNES   SENSE2            TO ESTABLISHE
012ER  2034                     169           BNES   SENSE2            TO ESTBLISH DATA LINK
0130R  C200 020AR               170           LPSW   WAIT
                                171  *
```

REMOTE TERMINAL DATA TRANSFER (16-BIT)

```
0134R  9F78                172  INT3    AIR   DEV,STAT
0136R  0572                173           CLHR  DEV,RCV
0138R  4230 0138R          174           BNE   *
013CR  C580 0008           175           CLHI  STAT,8          CARR OFF DROPS
0140R  4230 0140R          176           BNE   *
0144R  C850 0150R          177           LHI   WORK,INT4
0148R  4050 0046           178           STH   WORK,X'46'
014CR  C200 020AR          179  RDTEN   LPSW  WAIT
                           180  *
0150R  9F78                181  INT4    AIR   DEV,STAT
0152R  0572                182           CLHR  DEV,RCV
0154R  4230 0154R          183           BNE   *
0158R  0888                184           LHR   STAT,STAT       BSY DROPS WHEN KEY IS DEPRESSED
015AR  4230 015AR          185           BNZ   *
015ER  DB21 0000           186           RD    RCV,0(MSG)      READ CHARACTER INTO MESSAGE BUFFER
0162R  2611                187           AIS   MSG,1
0164R  C510 0244R          188           CLHI  MSG,MSG4END
0168R  4280 014CR          189           BL    RDTEN
                           190  *
016CR  C810 0238R          191           LHI   MSG,MSG3
0170R  DE30 0211R          192           OC    SND,ENWRT       SEND RQ2S
0174R  C850 0180R          193           LHI   WORK,INT5
0178R  4050 0046           194           STH   WORK,X'46'
017CR  C200 020AR          195  WRTEN   LPSW  WAIT
                           196  *
0180R  9F78                197  INT5    AIR   DEV,STAT
0182R  0573                198           CLHR  DEV,SND
0184R  4230 0184R          199           BNE   *
0188R  0888                200           LHR   STAT,STAT       CL2S NOT DROPS, BSY DROPS
018AR  4230 018AR          201           BNZ   *
018ER  0866                202           LHR   DONE,DONE
0190R  4230 01A8R          203           BNZ   DISCONN
0194R  DA31 0000           204           WD    SND,0(MSG)
0198R  2611                205           AIS   MSG,1
019AR  C510 024AR          206           CLHI  MSG,MSG3END
019ER  4280 017CR          207           BL    WRTEN
                           208  *
01A2R  2461                209           LIS   DONE,1
01A4R  4300 017CR          210           B     WRTEN           CLEAR LAST WRITE INT.
                           211  *
01A8R  C850 01B8R          212  DISCONN LHI   WORK,INT6
01ACR  4050 0046           213           STH   WORK,X'46'
01B0R  DE20 0216R          214           OC    RCV,DTROFF      DTR IS OFF TO DISCONNECT
01B4R  C200 020AR          215           LPSW  WAIT
                           216  *
01B8R  9F78                217  INT6    AIR   DEV,STAT
01BAR  0572                218           CLHR  DEV,RCV
01BCR  4230 01BCR          219           BNE   *
01C0R  C580 000C           220           CLHI  STAT,X'0C'      DSRDY DROP CAUSES AN INTERRUPT
01C4R  4230 01C4R          221           BNE   *
01C8R  C850 01D4R          222           LHI   WORK,INT7
01CCR  4050 0046           223           STH   WORK,X'46'
01D0R  C200 020AR          224           LPSW  WAIT
                           225  *
```

```
01D4R  9F78                 226  INT7     AIR    DEV,STAT
01D6R  0572                 227           CLHR   DEV,RCV
01D8R  4230 01D8R           228           BNE    *
01DCR  C580 000E            229           CLHI   STAT,X'0E'        CARR OFF SETS CAUSING AN INT.
01E0R  4230 01E0R           230           BNE    *
01E4R  C850 01F0R           231           LHI    WORK,INT8
01E8R  4050 0046            232           STH    WORK,X'46'
01ECR  C200 020AR           233           LPSW   WAIT
                            234  *
01F0R  9F78                 235  INT8     AIR    DEV,STAT
01F2R  0573                 236           CLHR   DEV,SND
01F4R  4230 01F4R           237           BNE    *
01F8R  C580 0048            238           CLHI   STAT,X'48'        CLOS NOT SETS, BSY IS ALSO SET
01FCR  4230 01FCR           239           BNE    *
0200R  4300 00B6R           240           B      HALT
                            241  *
                            242  * CONSTANTS & MESSAGES USED IN ABOVE EXAMPLES
                            243  *
0204R  0032                 244  RCVADR   DCX    32                PASLA (RECEIVE) ADDRESS
0206R  0033                 245  SNDADR   DCX    33                PASLA (SEND) ADDRESS
0208R  0010                 246  DEVADR   DCX    10                PASLA (HDX) ADDRESS
020AR  C000                 247  WAIT     DCX    C000              PSW FOR WAIT
020CR  00BER                248           DC     Z(START2)
020ER  78                   249  SECOND   DB     X'78'             PASLA SET UP FOR HIGHER BAUD RATE,
                            250  *                                 8 DATA BITS/CHAR, 2 STOP BITS,
                            251  *                                 NO PARITY CHECK.
020FR  AB                   252  DISWRT   DB     X'AB'             DISABLE INT, WRITE MODE
0210R  B9                   253  DISRD    DB     X'B9'             DISABLE INT, READ WITH ECHO-BACK
0211R  6B                   254  ENWRT    DB     X'6B'             ENABLE INT, WRITE MODE
0212R  83                   255  DISWRT2  DB     X'83'             DIS,WRITE
0213R  41                   256  ENREAD   DB     X'41'             EN,READ
0214R  03                   257  WRTRD    DB     X'03'             WRT/RD = 1
0215R  3B                   258  DTR      DB     X'3B'             DATA TERMINAL READY
0216R  03                   259  DTROFF   DB     X'03'             DTR = 0
                            260  *
0218R  54595045             261  MSG1     DC     C'TYPE 1234567890',X'0D0A'
       20313233
       34353637
       38393020
0228R  0D0A
       0000 022AR           262  MSG1END  EQU    *
       0000 021DR           263  TYPED    EQU    *-13
022AR  0D0A                 264  MSG2     DC     X'0D0A',C'CORRECT',X'2121',X'0D0A'
022CR  434F5252
       45435420
0234R  2121
0236R  0D0A
       0000 0238R           265  MSG2END  EQU    *
0238R  0D0A                 266  MSG3     DC     X'0D0A'
023AR                       267  MSG4     DS     10
       0000 0244R           268  MSG4END  EQU    *
0244R  0D0A                 269           DC     X'0D0A',0,0
0246R  0000
0248R  0000
```

```
     0000 024AR            270  MSG3END  EQU     *
                           271  *
024AR                      272           END
```

REMOTE TERMINAL DATA TRANSFER (16-BIT)

NO ERRORS 0 SQUEZ PASSES

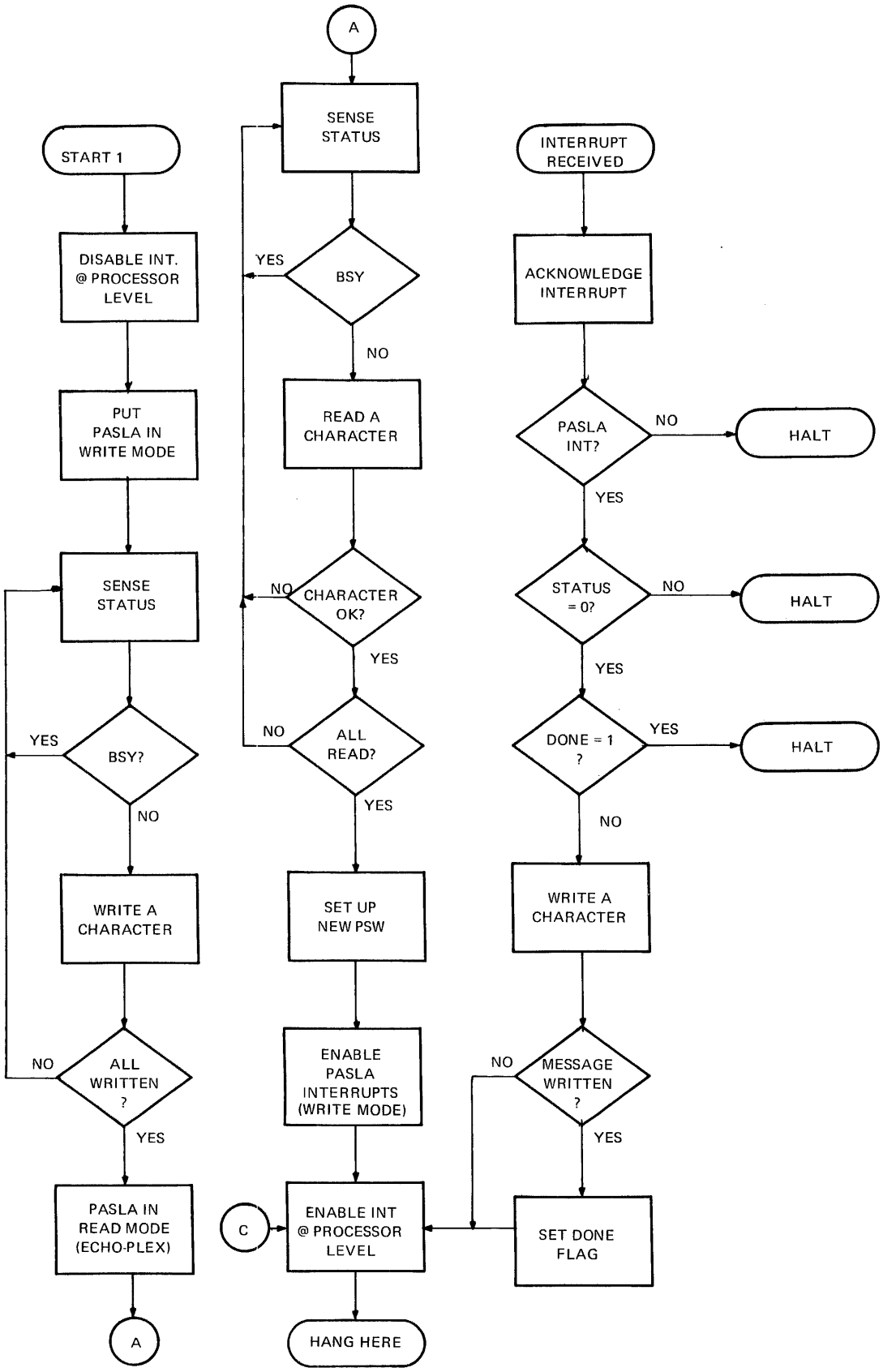
CALR03P

ABSTOP	0000												
ADC	0002												
BSY	0008	95	101 - 104										
CARRY	0006	109											
CHAR	0004	46	57	72	96	97	102						
DELAY	00AER	53	70										
DEV	0007	41	42	43	51	52	69	78	85	93	96	100	102	103
		157	158	172	173	181	182	197	198	217	218	226	227	235
		236												
DEVADR	0208R	41												
DISCONN	01A8R	203												
DISRD	0210R	51												
DISWRT	020FR	43												
DISWRT2	0212R	141												
DONE	0006	38	38	39	66	82	82	89	132	132	133	135	202	202
		209												
DTR	0215R	162												
DTROFF	0216R	214												
ENREAD	0213R	146												
ENWRT	0211R	69	192											
EX	0004	94												
EXMP1A	0018R	50												
EXMP1B	0034R	61												
EXMP1C	0060R	88	90											
HALT	00B6R	83	94	240										
IMPTOP	024AR													
INT	006AR	65												
INT1	010AR	134												
INT3	0134R	163												
INT4	0150R	177												
INT5	0180R	193												
INT6	01B8R	212												
INT7	01D4R	222												
INT8	01F0R	231												
LADC	0001													
LINK	000F	47	53	56	70	98	105	110						
MSG	0001	44	46	48	49	54	54	57	59	60	68	85	86	87
		114	133	134	136	154	186	187	188	191	204	205	206	
MSG1	0218R	44												
MSG1END	022AR	49												
MSG2	022AR	68												
MSG2END	0238R	87												
MSG3	0238R	191												
MSG3END	024AR	206												
MSG4	023AR	154												
MSG4END	0244R	188												
OUTCHR	00A2R	47												
PURETOP	0000R													
RCV	0002	138	140	146	147	148	149	158	162	166	173	182	186	214
		218	227											

REMOTE TERMINAL DATA TRANSFER (16-BIT)

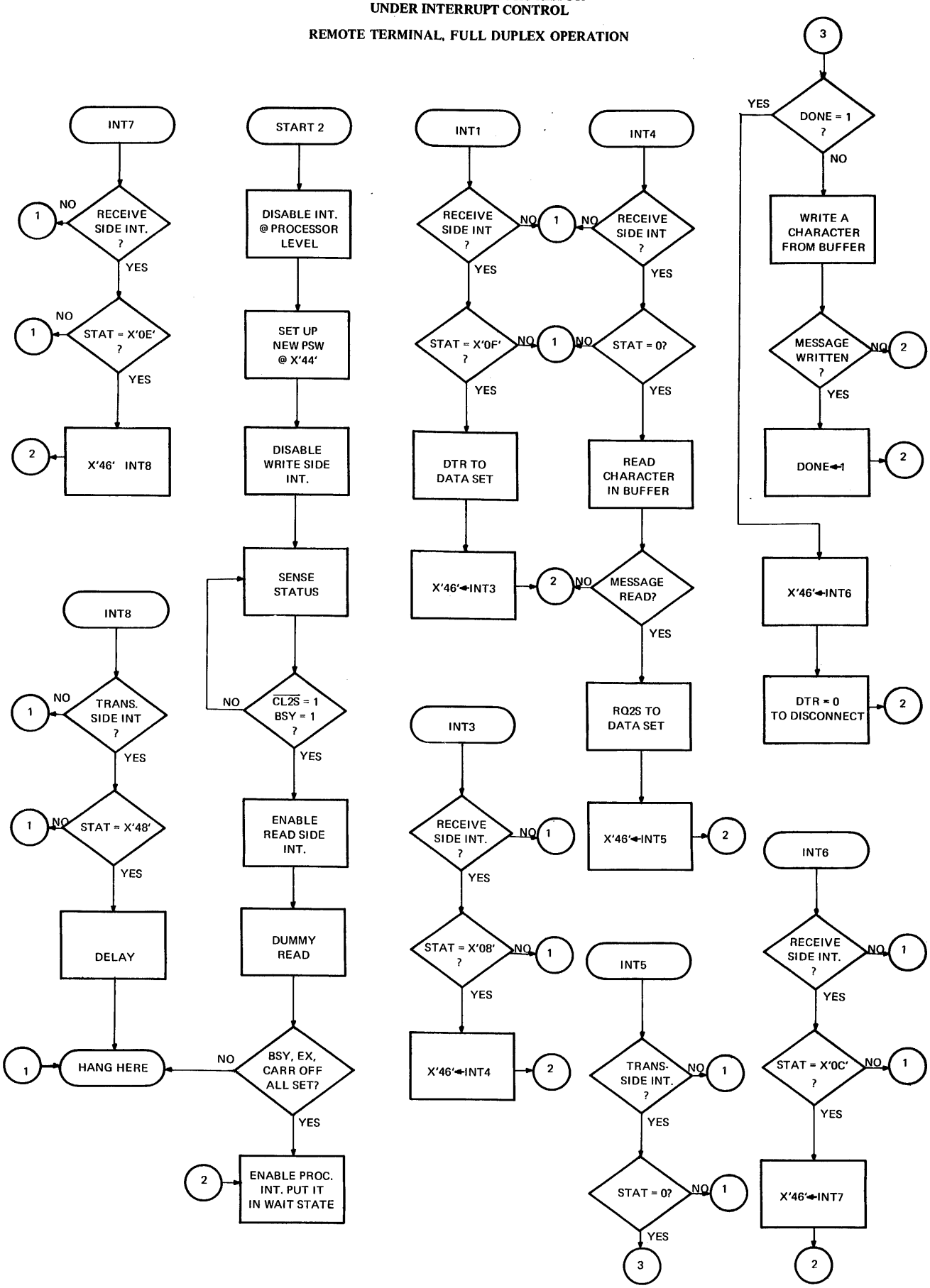
FLOW CHART FOR PASLA PROGRAMMING
EXAMPLE FOR 16-BIT PROCESSORS
USING SENSE STATUS LOOPS

LOCAL TERMINAL, HALF DUPLEX OPERATION



FLOW CHART FOR PASLA PROGRAMMING EXAMPLES FOR 16-BIT PROCESSOR UNDER INTERRUPT CONTROL

REMOTE TERMINAL, FULL DUPLEX OPERATION



PROG= *NONE* 03-066R03M96

```
                                1          SCRAT
                                2          CROSS
                                3          WIDTH  120
                                4          TARGT  32
                                5          NORX3
                                6  *
                                7  *
                                8  *  USER INPUTS A MESSAGE OF UP TO 72 CHARACTERS THROUGH THE TERMINAL
                                9  *  HOOKED ON TO THE PASLA INTERFACE. A MESSAGE OF LESS THAN 72
                               10  *  CHARACTERS MUST BE TERMINATED BY DEPRESSING 'CR' KEY TWICE. THE
                               11  *  AUTO-DRIVER CHANNEL READS THE CHARACTERS & DOES ASCII TO ASCII
                               12  *  TRANSLATION, AND GENERATES A BUFFER CALLED 'MESSAGE'.
                               13  *  THEN CCB IS SET UP TO WRITE, FAST MODE, NO TRANSLATION. THE
                               14  *  'CR', 'LF' OR JUST 'LF' IS OUTPUT FOLLOWED BY THE 'MESSAGE'
                               15  *  BUFFER. THEN 'CR', 'LF' ARE OUTPUT.
                               16  *
                               17  *  THE ENTIRE PROGRAM LOOPS ON ITSELF.
                               18  *
                               19  *
                               20  * REGISTER EQUATES
                               21  *
                               22  *
0000 0000                      23  R0      EQU    0
0000 0001                      24  R1      EQU    1
0000 0007                      25  DEV     EQU    7
0000 000A                      26  WORK    EQU    10
```

DATA TRANSFER THROUGH AUTO-DRIVER CHANNEL


```
                                    28  *
0000001                             29          ORG     X'A00'
                                    30  *
                                    31  *
000A00   C810 00F0                  32  START1  LHI     R1,X'F0'
000A04   9501                       33          EPSR    R0,R1               REGISTER SET F
                                    34  *
000A06   4870 0BB2                  35          LH      DEV,RCVADR          GET RECEIVE SIDE ADDRESS
000A0A   9B7A                       36          RDR     DEV,WORK            DUMMY READ TO SET BUSY
000A0C   4070 0BB0                  37          STH     DEV,DEVADR
                                    38  *
000A10   C810 F702                  39          LHI     R1,CCWSTA+TLATE
000A14   4010 0B48                  40          STH     R1,CCW              LRC, BUFFER 0, READ, TRANSLATE
000A18   E610 0BA7                  41          LDAI    R1,RBUF0END
000A1C   E600 0B60                  42          LDAI    R0,MESSAGE
000A20   0B01                       43          SAR     R0,R1
000A22   4000 0B4A                  44          STH     R0,COUNT0
000A26   5010 0B4C                  45          STA     R1,BUF0END
000A2A   D300 0EA2                  46          LB      R0,ENREAD           GET READ COMMAND
000A2E   D200 0BB4                  47          STB     R0,CMD
000A32   24A1                       48          LIS     WORK,1
000A34   40A0 0BAC                  49          STH     WORK,READ           SET FLAG
                                    50  *
000A38   C810 0B48                  51  COMM    LHI     R1,CCB
000A3C   2611                       52          AIS     R1,1
000A3E   4017 4700 00D0             53          STH     R1,ISPTAB(DEV,DEV)  SET UP ISP TABLE ENTRY
000A44   2418                       54          LIS     R1,8
000A46   7610 0B48                  55          RBT     R1,CCW              RESET EX BIT
000A4A   C810 0AAC                  56          LHI     R1,ISR0
000A4E   4010 0B5C                  57          STH     R1,SUBR             SUBROUTINE ADDRESS
                                    58  *
000A52   C810 40F0                  59          LHI     R1,X'40F0'
000A56   9501                       60          EPSR    R0,R1               ENABLE INT @ PROCESSOR LEVEL
000A58   4870 0BB0                  61          LH      DEV,DEVADR
000A5C   E207 0000                  62          SINT    0(DEV)
000A60   4300 0A60                  63          B       *                   HANG
                                    64  *
                                    65  *  TO WRITE CR, LF OR JUST LF FOLLOWED BY MESSAGE & CR, LF.
                                    66  *
000A64   0700                       67  CRFXIT  XAR     R0,R0
000A66   4810 0B4A                  68          LH      R1,COUNT0
000A6A   CA10 0048                  69          AHI     R1,72
000A6E   0B01                       70          SAR     R0,R1
000A70   FA10 0000 0B5E             71          AAI     R1,WRTBUF
000A76   2306                       72          BS      OK
000A78   E610 0BA7                  73  LINEXIT LDAI    R1,RBUF0END
000A7C   E600 0B5E                  74          LDAI    R0,WRTBUF
000A80   0B01                       75          SAR     R0,R1
000A82   4000 0B4A                  76  OK      STH     R0,COUNT0
000A86   5010 0B4C                  77          STA     R1,BUF0END
000A8A   C810 F704                  78          LHI     R1,CCWSTA+WRITE     WRITE, NO TRANSLATION
000A8E   4010 0B48                  79          STH     R1,CCW
000A92   D300 0EA6                  80          LB      R0,ENWRT
000A96   D200 0BB4                  81          STB     R0,CMD
```

DATA TRANSFER THROUGH AUTO-DRIVER CHANNEL

```
000A9A  4870 0EA0   82          LH      DEV,SNDADR
000A9E  4070 0BB0   83          STH     DEV,DEVADR
000AA2  07AA        84          XAR     WORK,WORK
000AA4  40A0 0BAC   85          STH     WORK,READ           RESET FLAG
000AA8  4300 0A38   86          B       COMM
                    87  *
                    88  *  COME HERE AFTER SINT
                    89  *
000AAC  42F0 0AAC   90  ISR0    BTC     C+V+G+L,*
000AB0  C330 0008   91          THI     3,8
000AB4  4330 0A00   92          BZ      START1
000AB8  DE20 0EA7   93          OC      2,SECOND            SET UP PASLA
000ABC  DE20 0BB4   94          OC      2,CMD               ISSUE COMMAND
000AC0  48A0 0BAC   95          LH      WORK,READ
000AC4  4330 0AD4   96          BZ      ISR01
000AC8  9B2A        97          RDR     2,WORK              SET BSY
000ACA  E6A0 0AE4   98          LDAI    WORK,ISR1
000ACE  40A0 0B5C   99          STH     WORK,SUBR           TO READ A MESSAGE
000AD2  1800       100          LPSWR   R0
                   101  *
000AD4  E6A0 0BC4  102  ISR01   LDAI    WORK,ISR2
000AD8  40A0 0B5C  103          STH     WORK,SUBR           TO WRITE THE MESSAGE
000ADC  24A8       104          LIS     WORK,8
000ADE  75A0 0B48  105          SBT     WORK,CCW            SET EX BIT
000AE2  1800       106          LPSWR   R0
                   107  *
                   108  * COME HERE TO READ FIRST CHARACTER
                   109  *
000AE4  42F0 0AE4  110  ISR1    BTC     C+V+G+L,*
000AE8  C330 0008  111          THI     3,8
000AEC  4230 0A00  112          BNZ     START1
000AF0  9B2A       113          RDR     2,WORK              READ FIRST CHARACTER OF MESSAGE
000AF2  E3A0 0B48  114          SCP     WORK,CCB            PUT IT IN BUFFER
000AF6  4300 0AD4  115          B       ISR01
                   116  *
                   117  *
000AFA  1800       118  IGNORE  LPSWR   R0
                   119  *
                   120  *
000AFC  07AA       121  CR      XAR     WORK,WORK
000AFE  40A0 0B48  122          STH     WORK,CCW            RESET EXE BIT
000B02  1800       123          LPSWR   R0
                   124  *
                   125  *
                   126  *  COME HERE AFTER ADC TERMINATION
                   127  *
000B04  4210 0B04  128  ISR2    BTC     L,*
000B08  4220 0B18  129          BTC     G,BUFULL
000B0C  48A0 0BAC  130          LH      WORK,READ
000B10  4330 0B10  131          BZ      *
000B14  4300 0A64  132          B       CREXIT
000B18  48A0 0BAC  133  BUFULL  LH      WORK,READ
000B1C  4230 0A78  134          BNZ     LINEXIT
000B20  C8A0 FFFD  135          LHI     WORK,-3             TO OUTPUT CR, LF, NULL, NULL.
```

```
000B24  40A0 0B52          136           STH     WORK,COUNT1
000B28  E6A0 0BAB          137           LDAI    WORK,WBUF1END
000B2C  50A0 0B54          138           STA     WORK,BUF1END
000B30  C8A0 0B3A          139           LHI     WORK,IODONE
000B34  40A0 0B5C          140           STH     WORK,SUBR
000B38  1800               141           LPSWR   R0
                           142   *
                           143   *  COME HERE WHEN ALL I/O OPERATION IS OVER
                           144   *
                           145   *
000B3A  4210 0B3A          146   IODONE  BTC     L,*
000B3E  4220 0A00          147           BTC     G,START1
000B42  4300 0B42          148           B       *
                           149   *
000B48                     150           ALIGN   ADC
                           151   *-------------------------------
                           152   *
        0000 0B48          153   CCB     EQU     *
000B48  0000               154   CCW     DCX     0
000B4A  0000               155   COUNT0  DCX     0
000B4C  0000 0000          156   BUF0END DC      0
000B50  0000               157   CHKWORD DCX     0
000B52  0000               158   COUNT1  DCX     0
000B54  0000 0000          159   BUF1END DC      0
000B58  0000 0BB8          160           DC      A(TLATETAB)
000B5C  0000               161   SUBR    DCX     0
                           162   *
                           163   *-------------------------------
                           164   *  BUFFERS
                           165   *
000B5E  0D                 166   WRTBUF  DB      13
000B5F  0A                 167           DB      10
000B60                     168   MESSAGE DS      72
        0000 0BA7          169   RBUF0END EQU    *-1
000BA8  0D0A               170           DCX     0D0A,0
000BAA  0000
        0000 0BAB          171   WBUF1END EQU    *-1
                           172   *-------------------------------
                           173   *
                           174   *  EQUATES
                           175   *
        0000 F700          176   CCWSTA  EQU     X'F700'
        0000 0004          177   WRITE   EQU     X'0004'
        0000 0002          178   TLATE   EQU     X'0002'
                           179   *
        0000 00D0          180   ISPTAB  EQU     X'D0'
        0000 0008          181   C       EQU     8
        0000 0004          182   V       EQU     4
        0000 0002          183   G       EQU     2
        0000 0001          184   L       EQU     1
                           185   *
                           186   *
                           187   *  CONSTANTS
                           188   *
```

DATA TRANSFER THROUGH AUTO-DRIVER CHANNEL

```
                                  189  *
000BAC   0000 0000                190  READ     DC     0
000BB0   0000                     191  DEVADR   DCX    0
000BB2   0010                     192  RCVADR   DCX    10
000BB4   00                       193  CMD      DB     0
                                  194  *
                                  195  *--------------------------------
                                  196  *
000BB8                            197           ALIGN  ADC+ADC
                                  198  *
000BB8                            199  TLATETAB DO     13
000BB8   057D                     200           DC     T(IGNORE)
000BBA   057D                     200           DC     T(IGNORE)
000BBC   057D                     200           DC     T(IGNORE)
000BBE   057D                     200           DC     T(IGNORE)
000BC0   057D                     200           DC     T(IGNORE)
000BC2   057D                     200           DC     T(IGNORE)
000BC4   057D                     200           DC     T(IGNORE)
000BC6   057D                     200           DC     T(IGNORE)
000BC8   057D                     200           DC     T(IGNORE)
000BCA   057D                     200           DC     T(IGNORE)
000BCC   057D                     200           DC     T(IGNORE)
000BCE   057D                     200           DC     T(IGNORE)
000BD0   057D                     200           DC     T(IGNORE)
000BD2   057E                     201           DC     T(CR)
000BD4                            202           DO     9
000BD4   057D                     203           DC     T(IGNORE),T(IGNORE)
000BD6   057D
000BD8   057D                     203           DC     T(IGNORE),T(IGNORE)
000BDA   057D
000BDC   057D                     203           DC     T(IGNORE),T(IGNORE)
000BDE   057D
000BE0   057D                     203           DC     T(IGNORE),T(IGNORE)
000BE2   057D
000BE4   057D                     203           DC     T(IGNORE),T(IGNORE)
000BE6   057D
000BE8   057D                     203           DC     T(IGNORE),T(IGNORE)
000BEA   057D
000BEC   057D                     203           DC     T(IGNORE),T(IGNORE)
000BEE   057D
000BF0   057D                     203           DC     T(IGNORE),T(IGNORE)
000BF2   057D
000BF4   057D                     203           DC     T(IGNORE),T(IGNORE)
000BF6   057D
         0000 0BF8                204  TABLE    EQU    *
000BF8                            205           DO     32
000BF8   80208021                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000BFC   80228023                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C00   80248025                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C04   80268027                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C08   80288029                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C0C   802A802B                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C10   802C802D                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C14   802E802F                 206           DB     X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
```

```
000C18  80308031          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C1C  80328033          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C20  80348035          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C24  80368037          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C28  80388039          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C2C  803A803B          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C30  803C803D          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C34  803E803F          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C38  80408041          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C3C  80428043          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C40  80448045          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C44  80468047          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C48  80488049          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C4C  804A804B          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C50  804C804D          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C54  804E804F          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C58  80508051          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C5C  80528053          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C60  80548055          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C64  80568057          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C68  80588059          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C6C  805A805B          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C70  805C805D          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C74  805E805F          206          DB      X'80',*-TABLE+63/2,X'80',*-TABLE+63/2
000C78                    207          DO      16
000C78  057D              208          DC      T(IGNORE),T(IGNORE)
000C7A  057D
000C7C  057D              208          DC      T(IGNORE),T(IGNORE)
000C7E  057D
000C80  057D              208          DC      T(IGNORE),T(IGNORE)
000C82  057D
000C84  057D              208          DC      T(IGNORE),T(IGNORE)
000C86  057D
000C88  057D              208          DC      T(IGNORE),T(IGNORE)
000C8A  057D
000C8C  057D              208          DC      T(IGNORE),T(IGNORE)
000C8E  057D
000C90  057D              208          DC      T(IGNORE),T(IGNORE)
000C92  057D
000C94  057D              208          DC      T(IGNORE),T(IGNORE)
000C96  057D
000C98  057D              208          DC      T(IGNORE),T(IGNORE)
000C9A  057D
000C9C  057D              208          DC      T(IGNORE),T(IGNORE)
000C9E  057D
000CA0  057D              208          DC      T(IGNORE),T(IGNORE)
000CA2  057D
000CA4  057D              208          DC      T(IGNORE),T(IGNORE)
000CA6  057D
000CA8  057D              208          DC      T(IGNORE),T(IGNORE)
000CAA  057D
000CAC  057D              208          DC      T(IGNORE),T(IGNORE)
000CAE  057D
000CB0  057D              208          DC      T(IGNORE),T(IGNORE)
```

```
000CB2  057D
000CB4  057D                    208             DC      T(IGNORE),T(IGNORE)
000CB6  057D
                                209  *
                                210  *
000CB8                          211             DO      13
000CB8  057D                    212             DC      T(IGNORE)
000CBA  057D                    212             DC      T(IGNORE)
000CBC  057D                    212             DC      T(IGNORE)
000CBE  057D                    212             DC      T(IGNORE)
000CC0  057D                    212             DC      T(IGNORE)
000CC2  057D                    212             DC      T(IGNORE)
000CC4  057D                    212             DC      T(IGNORE)
000CC6  057D                    212             DC      T(IGNORE)
000CC8  057D                    212             DC      T(IGNORE)
000CCA  057D                    212             DC      T(IGNORE)
000CCC  057D                    212             DC      T(IGNORE)
000CCE  057D                    212             DC      T(IGNORE)
000CD0  057D                    212             DC      T(IGNORE)
000CD2  057E                    213             DC      T(CR)
000CD4                          214             DO      9
000CD4  057D                    215             DC      T(IGNORE),T(IGNORE)
000CD6  057D
000CD8  057D                    215             DC      T(IGNORE),T(IGNORE)
000CDA  057D
000CDC  057D                    215             DC      T(IGNORE),T(IGNORE)
000CDE  057D
000CE0  057D                    215             DC      T(IGNORE),T(IGNORE)
000CE2  057D
000CE4  057D                    215             DC      T(IGNORE),T(IGNORE)
000CE6  057D
000CE8  057D                    215             DC      T(IGNORE),T(IGNORE)
000CEA  057D
000CEC  057D                    215             DC      T(IGNORE),T(IGNORE)
000CEE  057D
000CF0  057D                    215             DC      T(IGNORE),T(IGNORE)
000CF2  057D
000CF4  057D                    215             DC      T(IGNORE),T(IGNORE)
000CF6  057D
        0000 0CF8               216  TABLEH    EQU     *
000CF8                          217             DO      32
000CF8  80208021                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000CFC  80228023                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D00  80248025                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D04  80268027                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D08  80288029                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D0C  802A802B                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D10  802C802D                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D14  802E802F                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D18  80308031                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D1C  80328033                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D20  80348035                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D24  80368037                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D28  80388039                218             DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
```

```
000D2C  803A803B          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D30  803C803D          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D34  803E803F          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D38  80408041          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D3C  80428043          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D40  80448045          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D44  80468047          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D48  80488049          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D4C  804A804B          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D50  804C804D          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D54  804E804F          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D58  80508051          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D5C  80528053          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D60  80548055          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D64  80568057          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D68  80588059          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D6C  805A805B          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D70  805C805D          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D74  805E805F          218          DB      X'80',*-TABLEH+63/2,X'80',*-TABLEH+63/2
000D78                    219          DD      16
000D78  057D              220          DC      T(IGNORE),T(IGNORE)
000D7A  057D
000D7C  057D              220          DC      T(IGNORE),T(IGNORE)
000D7E  057D
000D80  057D              220          DC      T(IGNORE),T(IGNORE)
000D82  057D
000D84  057D              220          DC      T(IGNORE),T(IGNORE)
000D86  057D
000D88  057D              220          DC      T(IGNORE),T(IGNORE)
000D8A  057D
000D8C  057D              220          DC      T(IGNORE),T(IGNORE)
000D8E  057D
000D90  057D              220          DC      T(IGNORE),T(IGNORE)
000D92  057D
000D94  057D              220          DC      T(IGNORE),T(IGNORE)
000D96  057D
000D98  057D              220          DC      T(IGNORE),T(IGNORE)
000D9A  057D
000D9C  057D              220          DC      T(IGNORE),T(IGNORE)
000D9E  057D
000DA0  057D              220          DC      T(IGNORE),T(IGNORE)
000DA2  057D
000DA4  057D              220          DC      T(IGNORE),T(IGNORE)
000DA6  057D
000DA8  057D              220          DC      T(IGNORE),T(IGNORE)
000DAA  057D
000DAC  057D              220          DC      T(IGNORE),T(IGNORE)
000DAE  057D
000DB0  057D              220          DC      T(IGNORE),T(IGNORE)
000DB2  057D
000DB4  057D              220          DC      T(IGNORE),T(IGNORE)
000DB6  057D
```

LOCAL TERMINAL, FULL-DUPLEX PASLA OPERATION

```
                                  *
                                  *  THE TERMINAL SHOULD BE INTERFACED THROUGH PASLA(FDX) INTERFACE
                                  *  THE FOLLOWING EXAMPLE IS FOR 32-BIT PROCESSOR
                                  *  START EXECUTION @ START2
                                  *
                                  *  READ 10 KEYS & WRITE THOSE 10 CHARACTERS UNDER INTERRUPT CONTROL
                                  *
                                  *
                                  *  REGISTER ASSIGNMENTS
                                  *
     0000 0000                    DONE    EQU   0          EXAMPLE DONE FLAG
     0000 0002                    DEV0    EQU   2          PASLA (RECEIVE) ADDRESS
     0000 0003                    DEV1    EQU   3          PASLA (SEND) ADDRESS
     0000 0004                    MSG     EQU   4          MESSAGE ADDRESS
     0000 0005                    STAT    EQU   5          PASLA STATUS
     0000 000A                    R10     EQU   10         WORK REGISTER
     0000 000B                    R11     EQU   11         WORK REGISTER
     0000 000C                    R12     EQU   12         WORK REGISTER
     0000 0003                    R3      EQU   3          STATUS OF INTERRUPTING DEVICE
                                  *
     0000 0008                    BSY     EQU   8
                                  *
                                  *
000DB8  F8A0 0000 00F0            START2  LI    WORK,Y'F0'
000DBE  954A                              EPSR  MSG,WORK   NO INT, REG SET F
                                  *
                                  * SET UP INTERRUPT SERVICE POINTER TABLE
                                  *
000DC0  E640 0E98                         LDAI  MSG,HALT
000DC4  E6A0 00D0                         LDAI  R10,X'D0'
000DC8  24B2                              LIS   R11,2
000DCA  E6C0 02CE                         LDAI  R12,X'2CE'
000DCE  404A 0000                 EXMP2A  STH   MSG,0(R10) SET UP ENTIRE TABLE WITH 'HALT'
000DD2  C1AB 0DCE                         BXLE  R10,EXMP2A
                                  *
000DD6  4820 0E9E                         LH    DEV0,RECADR GET BOTH ADDRESSES
000DDA  4830 0EA0                         LH    DEV1,SNDADR
000DDE  DE20 0EA7                         OC    DEV0,SECOND SET UP PASLA
000DE2  08A2                              LR    R10,DEV0    SET UP 2 TABLE ENTRIES FOR
000DE4  0AAA                              AAR   R10,R10     RECEIVE & TRANSMIT DEVICES.
000DE6  C8A0 0E1A                         LHI   WORK,RECINT
000DEA  40AA 00D0                         STH   WORK,X'D0'(R10)
000DEE  08A3                              LR    R10,DEV1
000DF0  0AAA                              AAR   R10,R10
000DF2  C8A0 0E66                         LHI   WORK,SNDINT
000DF6  40AA 00D0                         STH   WORK,X'D0'(R10)
                                  *
000DFA  0700                      REPEAT2 XAR   DONE,DONE
000DFC  E640 0EAA                         LDAI  MSG,MSG33
000E00  4040 0E9C                         STH   MSG,READING RESET FLAG
000E04  DE20 0EA2                         OC    DEV0,ENREAD ENABLE READ SIDE INT, ECHO MODE
000E08  DE20 0EA5                         OC    DEV0,RQ2S
000E0C  9B2A                              RDR   DEV0,WORK   DUMMY READ TO SET BSY
000E0E  F8A0 0000 C0F0            EXMP2B  LI    WORK,Y'C0F0' ENABLE INT & HALT TTY DEPRESSION
```

```
000E14  95AA                    276             EPSR    R10,WORK        OF A KEY INTERRUPTS
000E16  4300 0E16               277             B       *
                                278     *
                                279     * RECEIVE SIDE HAS INTERRUPTED
                                280     *
000E1A  48A0 0E9C               281     RECINT  LH      R10,READING     HALT IF RECEIVE SIDE INTERRUPTS
000E1E  4330 0E1E               282             BZ      *               WHEN 'READING' FLAG IS RESET
000E22  0833                    283             LR      R3,R3           (R3) = RECEIVE SIDE STATUS
000E24  4230 0E24               284             BNZ     *               HALT IF NOT ZERO
000E28  F8A0 0000 00F0          285             LI      WORK,Y'F0'
000E2E  95AA                    286             EPSR    R10,WORK        REGISTER SET F
000E30  DB24 0000               287             RD      DEV0,0(MSG)     READ BYTE INTO MESSAGE BUFFER
000E34  2641                    288             AIS     MSG,1
000E36  F540 0000 0EB4          289             CLAI    MSG,MSG33END
000E3C  4280 0E0E               290             BL      EXMP2B          LOOP TILL 10 KEYS ARE READ IN.
                                291     *
                                292     * TO WRITE THE MESSAGE JUST READ IN
                                293     *
000E40  DE20 0EA3               294             OC      DEV0,DISRD      DISABLE READ SIDE INTERRUPTS
000E44  DE20 0EA5               295             OC      DEV0,RQ2S
000E48  E640 0EA8               296             LDAI    MSG,MSG3
000E4C  4000 0E9C               297             STH     DONE,READING    RESET FLAG
000E50  DE30 0EA6               298             OC      DEV1,ENWRT      ENABLE WRITE SIDE INTERRUPTS
000E54  9D35                    299             SSR     DEV1,STAT
000E56  2081                    300             BTBS    BSY,1
000E58  9A30                    301             WDR     DEV1,DONE       WRITE NULL TO GENERATE FIRST INT.
000E5A  F8A0 0000 C0F0          302     EXMP2C  LI      WORK,Y'C0F0'
000E60  95AA                    303             EPSR    R10,WORK        ENABLE INT @ PROCESSOR LEVEL & HALT
000E62  4300 0E62               304             B       *
                                305     *
                                306     * TRANSMIT SIDE HAS INTERRUPTED
                                307     *
000E66  48A0 0E9C               308     SNDINT  LH      R10,READING
000E6A  4230 0E6A               309             BNZ     *
000E6E  0833                    310             LR      R3,R3           STATUS SHOULD BE ZERO
000E70  4230 0E70               311             BNZ     *
000E74  F8A0 0000 00F0          312             LI      WORK,Y'F0'
000E7A  95AA                    313             EPSR    R10,WORK        REGISTER SET F
000E7C  0800                    314             LR      DONE,DONE
000E7E  4230 0DFA               315             BNZ     REPEAT2
000E82  DA34 0000               316             WD      DEV1,0(MSG)
000E86  2641                    317             AIS     MSG,1
000E88  F540 0000 0EB8          318             CLAI    MSG,MSG3END
000E8E  4280 0E5A               319             BL      EXMP2C
000E92  2401                    320             LIS     DONE,1
000E94  4300 0E5A               321             B       EXMP2C          TO CLEAR LAST WRITE INT
                                322     *
000E98  4300 0E98               323     HALT    B       *
                                324     *
                                325     *
                                326     * CONSTANTS USED IN ABOVE EXAMPLES
                                327     *
000E9C  0000                    328     READING DCX     0               READ FLAG
000E9E  0010                    329     RECADR  DCX     10              PASLA (RECEIVE) ADDRESS
```

LOCAL TERMINAL, FULL-DUPLEX PASLA OPERATION

```
000EA0    0011                330  SNDADR   DCX    11              PASLA (SEND) ADDRESS
000EA2    79                  331  ENREAD   DB     X'79'           ENABLE,ECHO,READ
000EA3    B9                  332  DISRD    DB     X'B9'           DISABLE,ECHO,READ
000EA4    AB                  333  DISWRT   DB     X'AB'           DISABLE,WRITE
000EA5    3B                  334  RQ2S     DB     X'3B'           REQUEST TO SEND (WRT/RD = 1)
000EA6    6B                  335  ENWRT    DB     X'6B'           ENABLE,WRITE
000EA7    78                  336  SECOND   DB     X'78'           HIGHER BAUD RATE, 8 BITS/CHAR,
                              337  *                               2 STOP BITS, NO PARITY CHECK
000EA8    0D0A                338  MSG3     DC     X'0D0A'
000EAA                        339  MSG33    DS     10              10 CHARACTER MESSAGE BUFFER
          0000 0EB4           340  MSG33END EQU    *
000EB4    0D0A                341           DC     X'0D0A'
000EB6    0000                342           DCX    0               2 NULL CHARACTERS
          0000 0EB8           343  MSG3END  EQU    *
                              344  *
000EB8                        345           END
```

LOCAL TERMINAL, FULL-DUPLEX PASLA OPERATION

NO ERRORS 0 SQUEZ PASSES

CALR03P

ABSTOP	0000 0ER8	
ADC	0000 0004	150 197 197
BSY	0000 0008	300
BUF0END	0000 0B4C	45 77
BUF1END	0000 0B54	138
BUFULL	0000 0B18	129
C	0000 0006	90 110
CCB	0000 0B48	51 114
CCW	0000 0B46	40 55 79 105 122
CCWSTA	0000 F700	39 78
CHKWORD	0000 0B50	
CMD	0000 0BB4	47 81 94
COMM	0000 0A38	86
COUNT0	0000 0B4A	44 68 76
COUNT1	0000 0B52	136
CR	0000 0AFC	201 213
CREXIT	0000 0A64	132
DEV	0000 0007	35 36 37 53 53 61 62 82 83
DEV0	0000 0002	257 259 260 272 273 274 287 294 295
DEV1	0000 0003	258 264 298 299 301 316
DEVADR	0000 0BB0	37 61 83
DISRD	0000 0EA3	294
DISWRT	0000 0EA4	
DONE	0000 0006	269 269 297 301 314 314 320
ENREAD	0000 0EA2	46 272
ENWRT	0000 0EA6	80 298
EXMP2A	0000 0DCE	255
EXMP2B	0000 0E0E	290
EXMP2C	0000 0E5A	319 321
G	0000 0002	90 110 129 147
HALT	0000 0E98	250
IGNORE	0000 0AFA	200 200 200 200 200 200 200 200 200 200 200 200 200
		203 203 203 203 203 203 203 203 203 203 203 203 203
		208 208 208 208 208 208 208 208 208 208 208 208 208
		208 208 208 208 208 208 208 208 208 208 208 208 208
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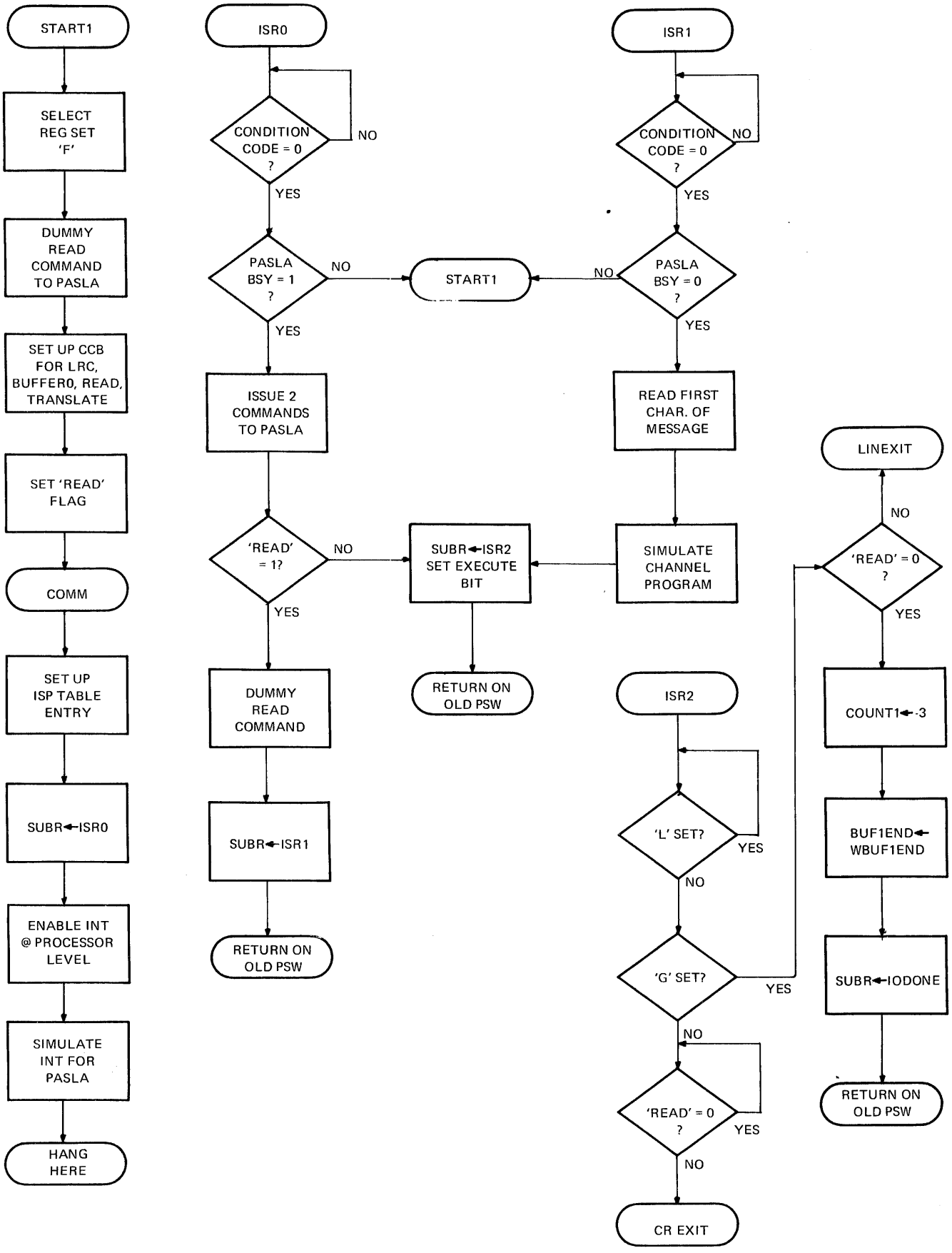
		215 215 215 215 215 215 215 215 215 215 215 215 215
		215 215 215 220 220 220 220 220 220 220 220 220 220
		220 220 220 220 220 220 220 220 220 220 220 220 220
IMPTOP	0000 0000I	
IODONE	0000 0B3A	139
ISPTAB	0000 00D0	53
ISR0	0000 0AAC	56
ISR01	0000 0AD4	96 115
ISR1	0000 0AE4	98
ISR2	0000 0B04	102
L	0000 0001	90 110 128 146
LADC	0000 0002	

FLOW CHART FOR PASLA PROGRAMMING
EXAMPLES FOR 32 BIT PROCESSORS
USING AUTO-DRIVER CHANNEL

LOCAL TERMINAL, FULL DUPLEX OPERATION



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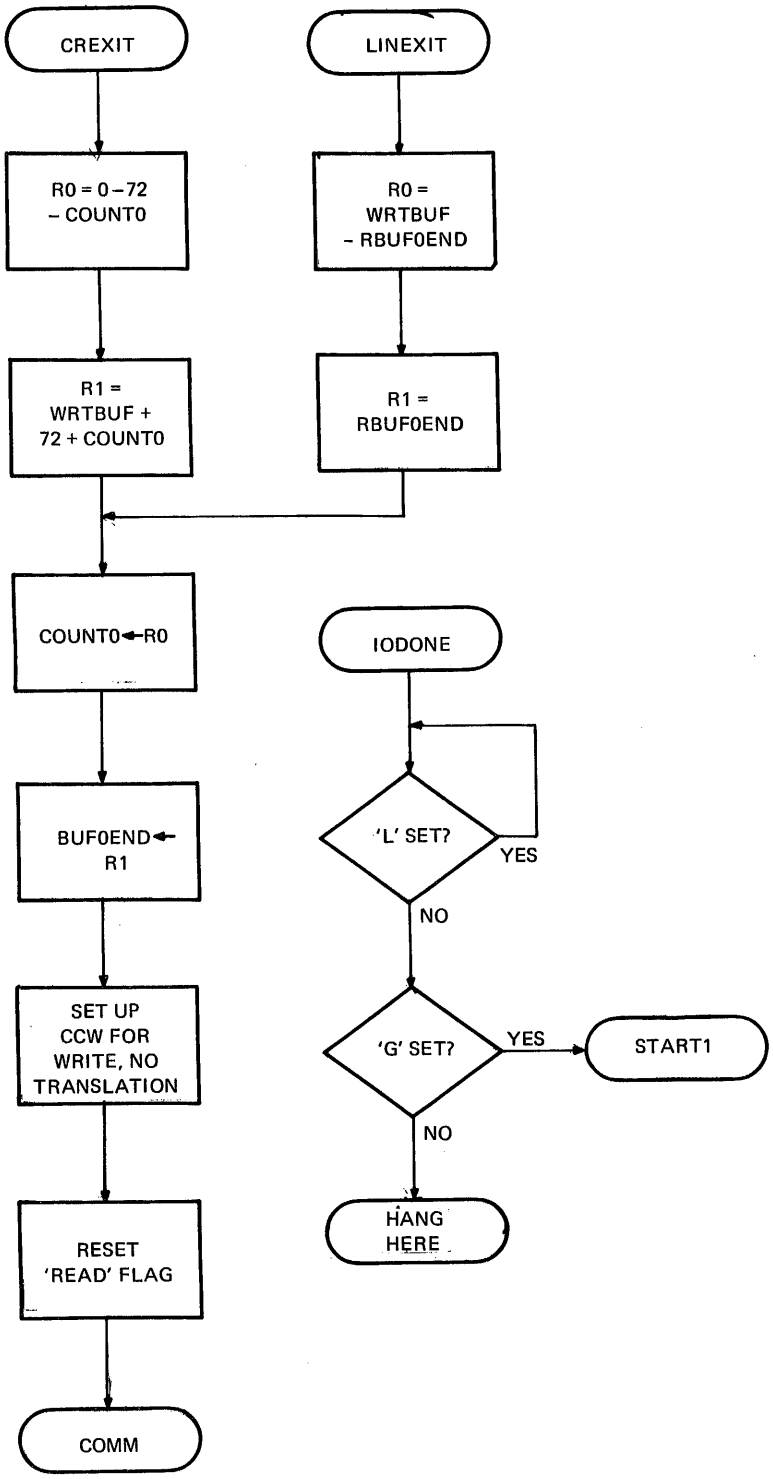
FOR 32 BIT PROCESSORS USING AUTO-DRIVER CHANNEL
(CONTINUED)



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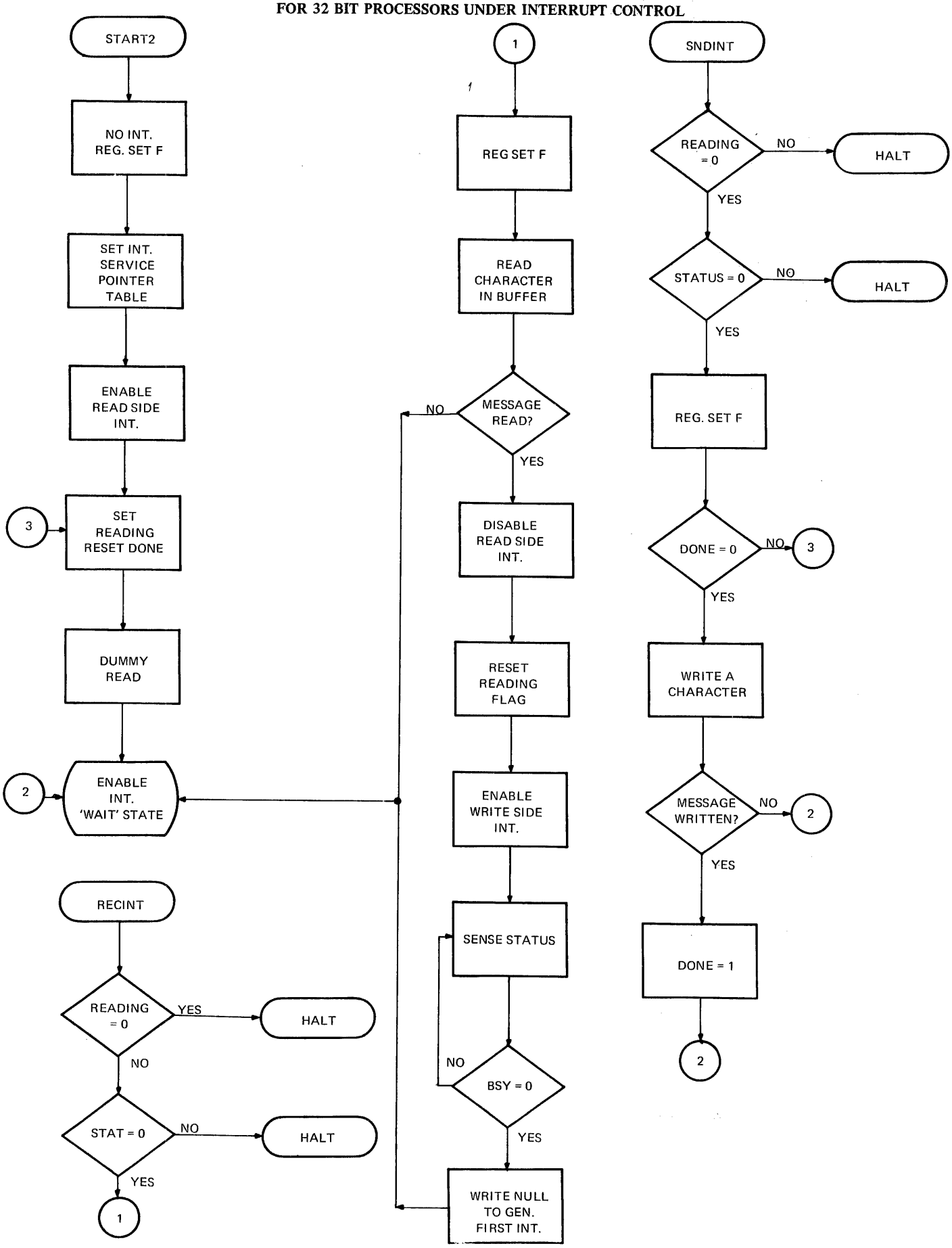

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